# PATMOS 2002

**Twelfth International Workshop on**
**Power And Timing Modeling, Optimization and Simulation**

September 11-13, 2002, Sevilla, Spain

http://www.patmos2002.org

IEEE CIRCUITS AND SYSTEMS SOCIETY Spanish Chapter

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## First CALL FOR PAPERS

Deadline: March 25, 2002

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**BACKGROUND:**

The workshop is the twelfth in a series of international workshops having been held in several places in Europe (visit the web site http://www.patmos-conf.org). PATMOS has over the years evolved into a well established and outstanding series of open European events on power and timing aspects of integrated circuit design. The increased interest, especially in low-power design, adds further momentum to the interest in this workshop. Despite its growth, the workshop can still be considered as an informal but very focused conference, featuring high-level scientific presentations together with open discussions and panel sessions in a free and easy environment. In the year 2002, the venue will be in Sevilla, Spain, organized by the Microelectronics Spanish Center (IMSE-CNM) and the University of Seville. Seville is the major city in the south-west of Spain and one of its richest historic, cultural and artistic spots.

**SCOPE:**

The objective of this workshop is to provide a forum to discuss and investigate the emerging problems in the design methodologies and CAD-tools for the new generation of IC technologies. A major emphasis of the technical program is on speed and low-power aspects with particular regard to modeling, characterization, design, and architectures. The scope of the workshop includes, but is not limited to design and CAD aspects of:

- Low power design: high performance low power systems, ultra low power systems, special architectures
- Modeling and synthesis: timing, power, low-voltage, interconnect, crosstalk
- Timing design: clocking, synchronization, asynchronous and self timed systems, adiabatic switching
- Optimization: low voltage low power logic families, logic parallelization, pipelining, fast low power arithmetic
- Physical design: module generation, library optimization and characterization, area estimation
- Physical test and characterization: low VT low voltage process, SOI, IDDQ, models and parameter extraction, experimental design for process control
- Design methods and CAD tools: for low voltage low power design, high speed circuits
- Trade-offs between devices, architectures and technologies, benchmark comparison

Contributions are invited for regular presentations and discussion sessions.
Prospective authors for regular presentations are invited to submit their complete paper including a 100-word abstract and illustrations in A4 camera ready format, not exceeding 10 pages. Electronic submission is required and should follow the style for the final publication. Check the web-page http://www.eivd.ch/patmos2001 for complete author and submission instructions. Submitted papers will be reviewed formally and anonymously by several reviewers.
Proposals for the panel sessions and special sessions are encouraged and must be received also not later than March 25, 2002.

**SCHEDULE:**

- Deadline for Submission of Paper: March 25, 2002
- Notification of Acceptance: May 31, 2002
- Deadline for Submission of Final Paper: June 21, 2002