Optimal charging of capacitors

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Abstract

Finite-time thermodynamics is illustrated by some examples of process optimalization. The objective is minimum entropy production during an electrical process, i.e. the charging of a capacitor. Non-linear electronic processes are investigated in particular, because of their importance in computers and displays.

1 Introduction

The problem is stated as follows: how to change the voltage $V_h(t)$ over a capacitor (with capacitance C) from an initially zero voltage (at time 0) to a final voltage V (at time τ) and how to discharge it subsequently? For this purpose we have to our disposal a voltage source $V_c(t)$. Between this source and the capacitor we assume an ohmic resistor (with conductance g). See Figure 1a.

The classical approach is as follows: the source consists of a constant voltage source V and an ideal switch. At $t = 0$ the switch is closed, such that the capacitor is connected to a voltage source $V_c(t) = V$. After sufficient time ($t \gg C/g$), the capacitor is charged: $V_h(t) \approx V$. See Figure 2a. The discharging happens analogously, the capacitor being connected to ground, i.e. to $V_c(t) = 0$. This classical strategy has two main disadvantages:

- In finite time the capacitor is not charged (or discharged) completely.
- The whole procedure (i.e. the complete charge-and-discharge cycle) costs an amount $\int g(V_c - V_h)^2 \, dt = CV^2$ of work, delivered by the voltage source and dissipated in the resistor ($\frac{1}{2}CV^2$ being dissipated during charging and $\frac{1}{2}CV^2$ during discharging). This amount is independent of g and thus applies also to the ideal case $g \to \infty$.

The work consumption and heat production are of great concern in two cases:

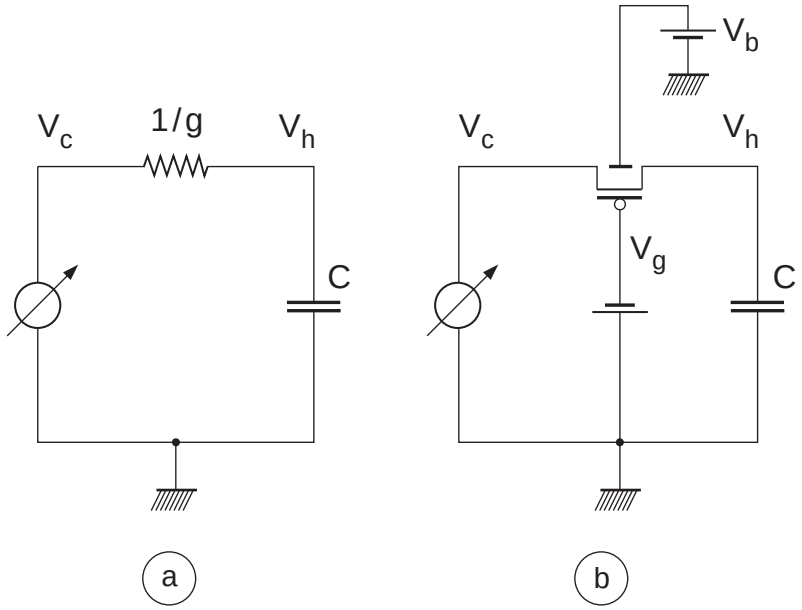

Figure 1: Electronic circuit: (a) with ohmic resistor, (b) with MOS transistor.

- In a digital computer, C is the capacitive load of a logic gate. Such a capacitor is frequently charged and discharged, because $V_h = V$ represents logic one, whereas $V_h = 0$ represents logic zero.
- In a flat display, C is the capacitance of a pixel. Such a capacitor is frequently charged and discharged, because $V_h = V$ realises 'light on', whereas $V_h = 0$ switches the light off [1].

The thousands of logic gates in a computer and the thousands of pixels on a display are source of a lot of concern:

- Computers (and displays) are the main energy consumers in several environments, such as offices, their heat dissipation often causing trouble for the people around.
- Portable equipment (such as 'lap tops') should consume as little as possible, in order to avoid too often replacement of the battery.
- Cooling of computer hardware is necessary in order to guarantee the reliability of the silicon circuits. The more we can avoid heating, the less we have to cool.

The problem is particularly interesting to treat in finite-time thermodynamics, because we are faced with very stringent conditions along the time axis. We have only a very fixed time τ to our disposal to (dis)charge the tiny capacitors. Indeed: computations are performed at a well defined and fixed pace, governed by the clock frequency; pictures are written at a well defined pace, governed by the frame rate. We can conclude that both in a computer and in a display, we have to charge and

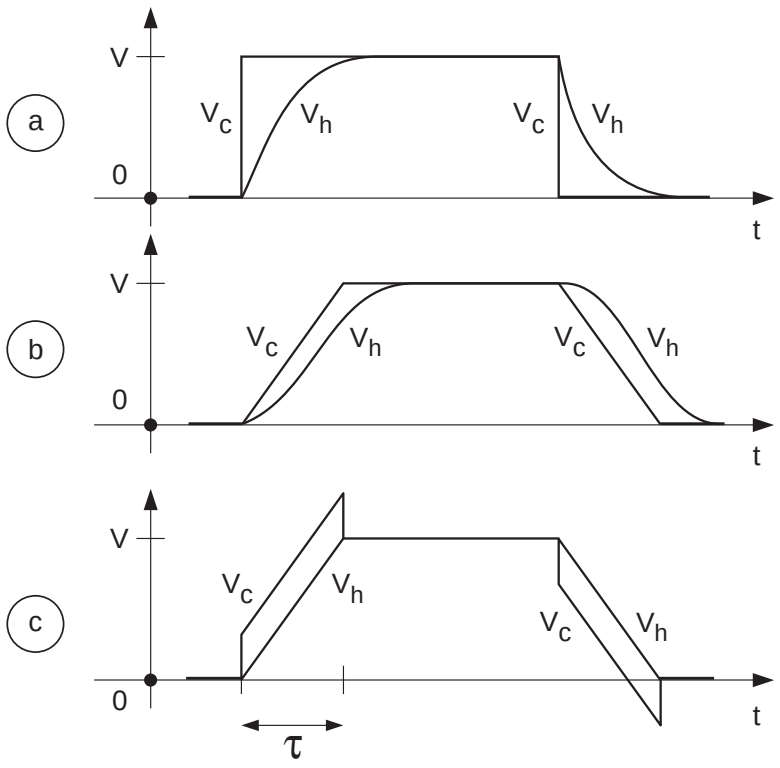

Figure 2: Time evolutions $V_c(t)$ and $V_h(t)$: (a) conventional 'step' strategy, (b) 'ramp' strategy, and (c) 'step + ramp' strategy.

discharge a huge number of small capacitors in a well defined but very short time, with a minimum of power dissipation. The challenge is the following: how to change the voltage source $V_c(t)$ in order to do better (i.e. to dissipate less) than the classical $\frac{1}{2}CV^2$?

In Section 2 we put the above problem within the framework of finite-time thermodynamics. In Section 3 an exact solution for the ohmic resistor model is given. Several strategies for the MOS transistor model are treated in Section 4.

2 Finite-time thermodynamics

We investigate the so-called *horse-and-carrot* problem [2]. The purpose is to move a 'carrot' in such a way that it attracts a 'horse' from one particular point to another, (a) in a well-defined time and (b) in an optimal way. Here we call a process 'optimal' if it generates a minimum amount of entropy:

$$S = \int_0^\tau \frac{dS}{dt}\, dt = \text{minimum} \ .$$

Here $\frac{dS}{dt}$ is the entropy creation rate. According to various authors, e.g. [2] [3], such process obeys $\frac{dS}{dt} =$ constant. For a single carrot and a single horse, we have

$$\frac{dS}{dt} = \sum_i \frac{dX_i}{dt}\ Z_i\ = \frac{dq}{dt}\ (\ -\frac{1}{T_c} + \frac{1}{T_h}\ ) + \frac{dN}{dt}\ (\ \frac{\mu_c}{T_c} - \frac{\mu_h}{T_h}\ ) + ...$$

where T_c, μ_c, ... are the temperature, chemical potential, ... of the carrot and T_h, μ_h, ... are the same intensive quantities for the horse. The flux $\frac{dq}{dt}$ is the heat flow from carrot to horse, $\frac{dN}{dt}$ is the particle flow from carrot to horse, ... Thus $\frac{dS}{dt} =$ constant becomes

$$\sum_i \frac{dX_i}{dt}\ Z_i = \text{ constant }. \tag{1}$$

According to Spirkl and Ries [4], this is only true provided the resistances to the driving forces as function of the fluxes are themselves independent of the fluxes. They propose the following (more general) rule:

$$\sum_{i,j}\ \frac{dX_i}{dt}\ \frac{\partial Z_i}{\partial \frac{dX_j}{dt}}\ \frac{dX_j}{dt} = \text{ constant }. \tag{2}$$

3 Model with ohmic resistor

In a purely electrical process, we have only one intensive variable, i.e. voltage V, and one extensive variable, i.e. charge Q. Entropy production obeys

$$\frac{dS}{dt} = \frac{dQ}{dt}\ (\ \frac{V_c}{T} - \frac{V_h}{T}\ )\ ,$$

where T is the temperature of both carrot and horse. First, we will restrict ourselves to the linear, i.e. ohmic, kinetic equation:

$$\frac{dQ}{dt} = g\ (V_c - V_h)\ ,$$

where g is a constant. We also have the relation $Q = f(V_h)$, where $f(x)$ is the (monotonously increasing) function describing the capacitance of the horse. Applying (1), i.e. $\frac{dQ}{dt} Z =$ constant, and applying (2), i.e. $\frac{dQ}{dt}\frac{\partial Z}{\partial \frac{dQ}{dt}}\frac{dQ}{dt} =$ constant, yield the same result:

$$\begin{aligned} & \frac{dQ}{dt} &=& \text{ constant }, \\ \text{and thus} \qquad & V_c - V_h &=& \text{ constant} \\ \text{or} \qquad & f'(V_h)\ \frac{dV_h}{dt} &=& \text{ constant }. \end{aligned}$$

For a linear capacitor (i.e. $f(x) = Cx$), together with the initial and final conditions $V_h(0) = 0$ and $V_h(\tau) = V$, this yields the following simple linear functions of time:

$$V_h(t) = V\ \frac{t}{\tau} \qquad \text{and} \qquad V_c(t) = V\ \frac{t}{\tau} + \frac{C}{g}\ \frac{V}{\tau}\ . \tag{3}$$

This result is not new: see [5] [6] [7]. Figure 2 shows the classical strategy (step), the quasi-optimal strategy (ramp), and finally the optimal strategy (step + ramp).

The power delivered by the voltage source is $\frac{dW}{dt} = V_c \frac{dQ}{dt}$. Therefore the work consumed during the optimal voltage rise is $W_{up} = \int_\tau \frac{dW}{dt} dt = \frac{1}{2} CV^2 + \frac{C^2V^2}{g\tau}$; the work consumed during the voltage decay is $W_{down} = -\frac{1}{2} CV^2 + \frac{C^2V^2}{g\tau}$. The total work during the whole cycle therefore is

$$W = 2 \frac{C^2V^2}{g\tau} . \tag{4}$$

For $\tau \gg C/g$, this energy, dissipated in the resistor, is much smaller than the energy CV^2. The limit $\tau \to \infty$ is called adiabatic charging-and-discharging [6] [8].

4 Model with MOS transistor

Unfortunately, an ohmic resistor is not an accurate model for a transistor. In Reference [9], we investigated various simple, but analytic, non-linear laws $\frac{dQ}{dt}$ as a function of V_c and V_h. As long as $\frac{dQ}{dt}$ is a function of V_c and V_h through the difference $V_c - V_h$ alone, the optimal strategy is $\frac{dQ}{dt} =$ constant.

Instead of an abstract non-linear resistor, in the present paper we take a MOS transistor (in our case a 2.4 μm $\times$ 7.2 μm p-MOS transistor, in the `Alcatel Microelectronics` n-well c-MOS 2.4 μm technology, with threshold voltage $V_t = -0.9$ V) to charge a $C = 37$ fF capacitor (i.e. the load formed by one n-MOS and one p-MOS transistor in parallel). Its current is a very complicated function of V_c (the source voltage) and V_h (the drain voltage), but also of the gate voltage (V_g), and even (but more weakly) of the bulk voltage (V_b). See Figure 1b. The complicated equivalent circuit contains, besides resistive elements, also capacitive elements. These laws are implemented into `HSpice`, where we use a `level 2` model.

Even for constant gate voltage V_g, the equations modeling the behaviour of the transistor do not allow us to solve for V_c and V_h as a function of Q and dQ/dt, such that we cannot write down an explicit analytical form for $Z(Q, \frac{dQ}{dt})$. Therefore, we will consider the transistor transport laws as a black box and try simple strategies.

4.1 First strategy

We first try the carrot voltage

$$V_c(t) = \frac{V}{\tau} t ,$$

i.e. the strategy of Figure 2b. We assume the gate is kept at constant voltage $V_g(t) = 0$, in order to keep the transistor switched on during the complete experiment.

As long as V_c is below the threshold voltage V_t, the source-gate voltage is too small to make the transistor conduct. Shortly after the moment that $V_c(t)$ equals V_t,

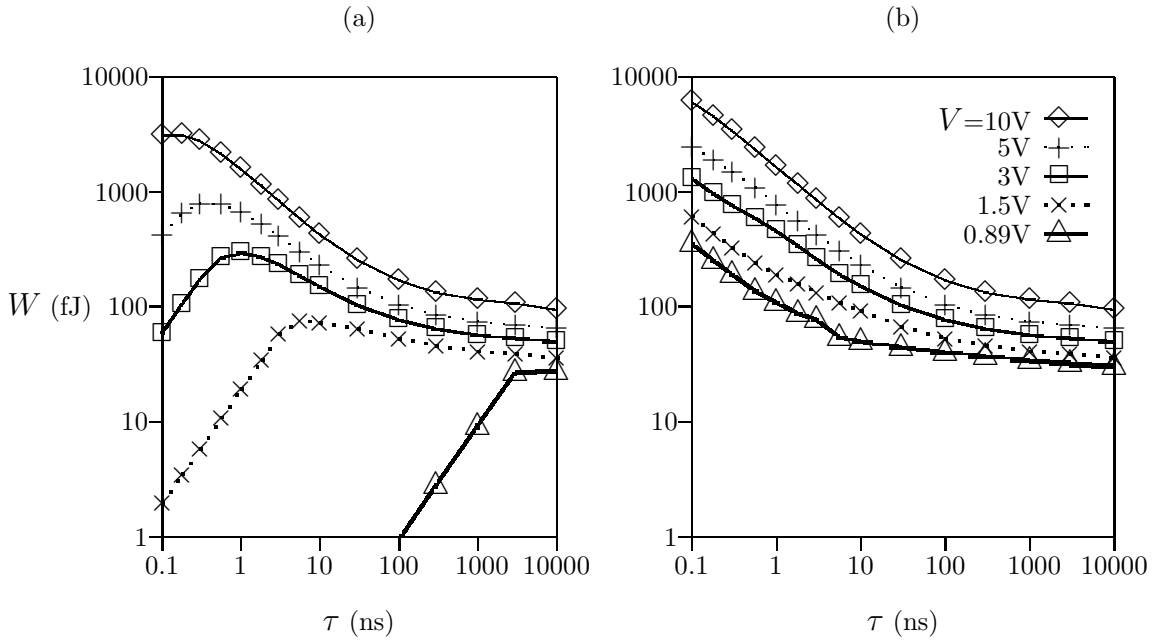

Figure 3: Energy consumption per charge-discharge cycle: (a) 'ramp' strategy, and (b) 'step + ramp' strategy.

the capacitor is suddenly connected to the source and thus quickly charged from 0 to V_c, i.e. approximately to V_t. During this charging an amount $\frac{1}{2}\,CV_t^2$ is dissipated. While V_c rises further from V_t to its final value V, further charging of the capacitor happens adiabatically. The first part of the discharging also happens 'smoothly', until V_c drops below V_t. Then the transistor is cut off and the capacitor cannot be discharged further. The remaining charge CV_t will subsequently be sent to ground voltage, resulting in the second $\frac{1}{2}\,CV_t^2$ dissipation.

The results of the numerical calculations show the dissipated energy W as a function of τ for various values of the voltage V to which the capacitor is to be charged. See Figure 3a. In order to interpret the results, let us look at the example $V = 5$ V.

- For $\tau = 0.3$ ns, dissipation per cycle is 789 fJ, i.e. close to the value $CV^2 =$ 925 fJ.
- For $\tau < 0.3$ ns, energy consumption is lower, but the capacitor voltage V_h is not able to follow the input signal V_c, such that the capacitor is not charged to the full 5 volts.
- For $\tau > 0.3$ ns, more precisely for 1 ns $\leq \tau \leq$ 10 ns, the energy consumption goes down like $\tau^{-0.49}$, i.e. slower than indicated by equation (4).
- For sufficiently long τ, the consumed energy W is about 65 fJ, i.e. somewhat above the expected value of $CV_t^2 = 30$ fJ.

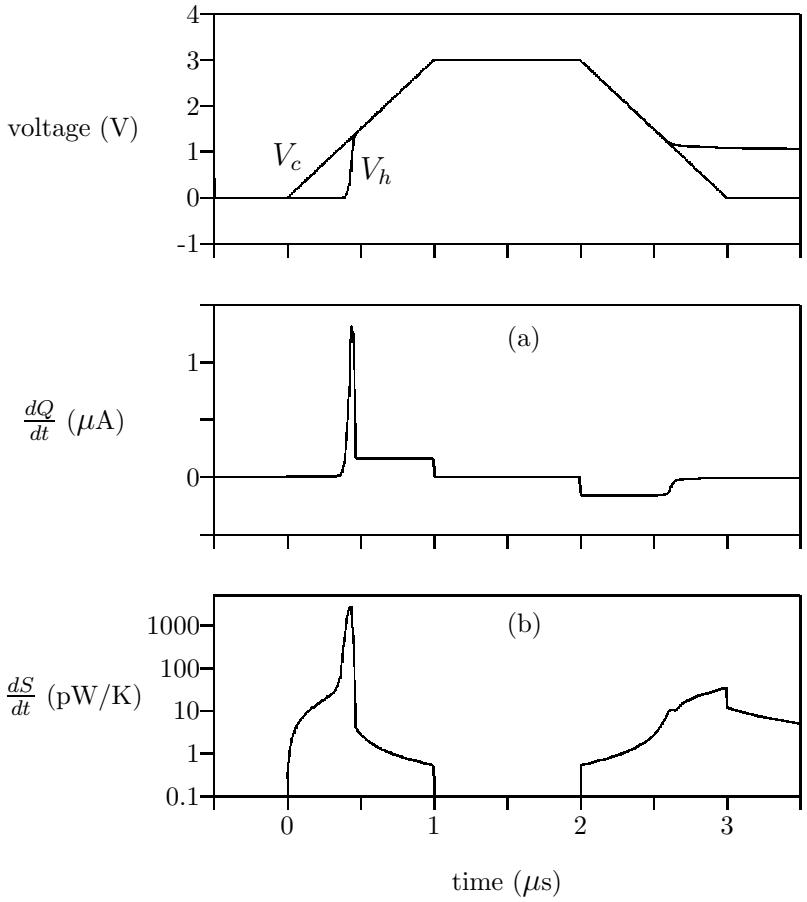

Figure 4: Variation of quantities during 'ramp' strategy: (a) electrical current, and (b) entropy production rate.

We remark that the curve $V = 0.89$ volts on Figure 3a illustrates the sub-threshold mode of the `HSpice` MOS-model. We see that in sub-threshold the circuit is extremely slow, due to the very high impedance of the MOS channel.

Note that the 'ramp' strategy is neither finite-time nor optimal. However, in order to demonstrate that the 'ramp' strategy is not that bad after all, Figure 4 shows the electrical current $\frac{dQ}{dt}$, as well as the entropy production rate $\frac{dQ}{dt}\, Z$, for the case $V = 3$ V and $\tau = 1$ μs. Apart from the zero current as long as $V_c < V_t$ and the peak shortly after $V_c = V_t$, the current is fairly constant, i.e. 162 nA during charging and $-$ 162 nA during discharging. The entropy creation rate is less constant: even if we again make abstraction of the peak following threshold, it varies between 1 and 20 pW/K. The 'Spirkl–Ries' quantity $\frac{dQ}{dt}\, \frac{\partial Z}{\partial \frac{dQ}{dt}}\, \frac{dQ}{dt}$ cannot be probed as a function of time by `HSpice`, because the MOS equations are not exclusively resistive.

4.2 Second strategy

Now we try the finite-time strategy

$$V_c(t) = \frac{V}{\tau}\ t + V_{step}\ , \tag{5}$$

i.e. the policy of Figure 2c. Here V_{step} is the step voltage added to the ramp voltage, in order to guarantee that $V_h(t)$ reaches its target value V after exactly the time τ. As the current-voltage laws of the transistor are unknown, we cannot apply a simple formula for V_{step}, such as the expression $\frac{CV}{g\tau}$ in eqn (3). On the contrary, for each value of the voltage V and the time τ, the step V_{step} has to be determined by 'trial-and-error' simulations, because the problem is of the 'split-boundary' type [5]. For V from 3 to 10 volts, it behaves more or less as τ^{-1}; for lower V, however, we find a much smaller slope of $V_{step}(\tau)$. Figure 3b shows the resulting energy dissipation. Note that for long τ these results scarcely differ from the results in Figure 3a, but for short τ we dissipate a larger amount of energy, i.e. the price we have to pay for calculating in finite time. We find more or less W proportional to $V^{1.1}\tau^{-0.55}$.

4.3 Third strategy

From qualitative studies on non-linear $\frac{dQ}{dt}$ transport laws [9], one can deduce that

$$V_c(t) = \begin{cases} V_{flat}\ , & t \le \frac{\tau}{V}\ (V_{flat} - V_{step}) \\ \frac{V}{\tau}\ t + V_{step}\ , & t \ge \frac{\tau}{V}\ (V_{flat} - V_{step}) \end{cases}$$

is a better strategy than (5). Indeed, `HSpice` reveals an energy gain by introducing a 'flat' carrot voltage before the linearly increasing ramp. Figure 5 shows the second and third strategy for the case $\tau = 1$ ns and $V = 3$ V, leading to 448 fJ and 421 fJ respectively. This result is new: the third strategy excels the second. However, the gain is modest, indicating that the second strategy is already close to optimum.

4.4 Further strategies

One could object that besides voltage source strategies, also electrical current strategies are possible. Replacing the time-dependent voltage source $V_c(t)$ by e.g. a constant current source would allow us to implement the '$\frac{dQ}{dt}$ = constant' strategy. However, it turns out that to impose a current to a MOS transistor often leads to problems, the current not flowing from the source pin to the drain pin, but instead to the bulk pin. Only a dramatic change of technology would avoid this problem. A possible candidate is SOI, i.e. silicon-on-insulator. It turns out that an SOI transistor would also allow lower V_t values, would get rid of leak currents to substrate, and would avoid the latch-up problem [10].

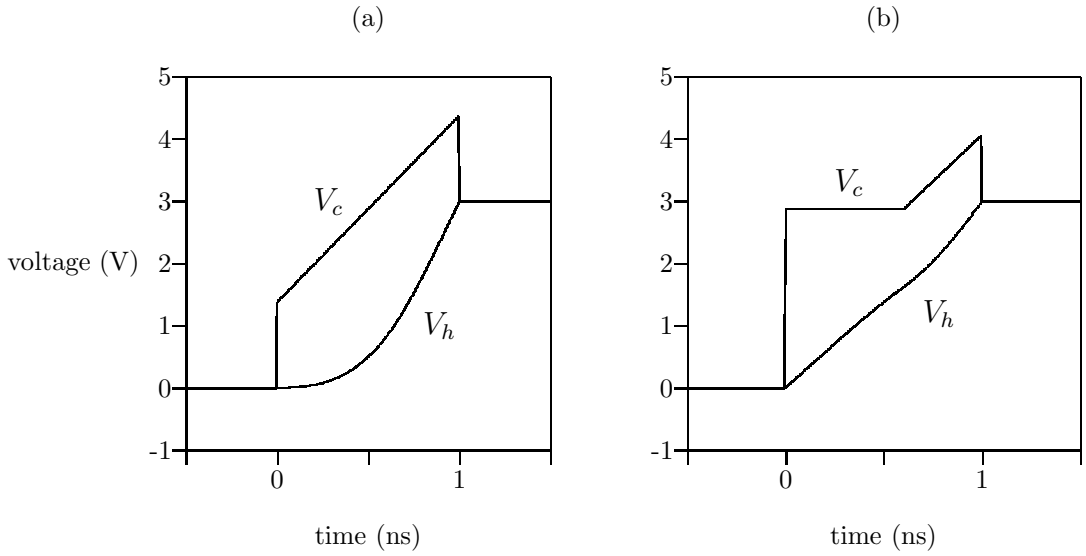

Figure 5: Time evolutions $V_c(t)$ and $V_h(t)$: (a) with the second strategy ($V_{step} = 1.38$ V), and (b) with the third strategy ($V_{flat} = 2.9$ V, $V_{step} = 1.07$ V).

New approaches would be most welcome in the framework of adiabatic computing. Indeed, further downscaling of present MOS technology leads to ever smaller capacitor values C, together with lower power supply voltages V and lower thresholds V_t, thus further lowering both dissipation quanta $\frac{1}{2}\ CV^2$ and $\frac{1}{2}\ CV_t^2$. The present roadmap of chip manufacturers foresees semiconductor fabrication processes designed for a proportional lowering of V and V_t, such that chips will keep on operating according to the rule of thumb $V_t \approx V/3$. This means that CV_t^2 will remain at about one tenth of CV^2 for the next years to come. It is not sure that a single order of magnitude gain is enough to convince designers of computer processors to consider applying adiabatic charging in their designs. Drastically new technologies, such as SOI, will probably lead to more substantial power reductions, making adiabatic switching sufficiently attractive.

5 Conclusion

Simple RC models for electrical systems can lead to explicit finite-time strategies, guaranteeing minimum entropy creation. Optimal trajectories can be calculated. Practical examples in electronics are not that easy to analyse, especially because a transistor current is a function of drain and source voltage, without being function of the voltage difference alone. As a consequence, pragmatic strategies have to replace optimal strategies.

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