Modeling the Effect of Wire Resistance in Deep Submicron Coupled Interconnects for Accurate Crosstalk Based Net Sorting

C. Guardiani, C. Forzan, B. Franzini, D. Pandini
Adanced Research, Central R&D, DAIS, STMicroelectronics,
via C.Olivetti, 2, I-20041 Agrate B., (MI), ITALY

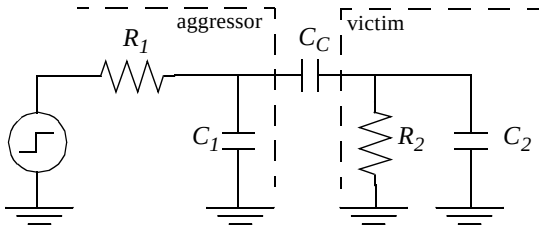
Abstract: It is well known that in deep submicron technologies the coupling capacitance between adjacent wires is a critical portion of the total wire capacitance, while at the same time the capacitance between wire and substrate has become the fringing component. High frequency signals travelling across multiple level interconnect structures generate proximity effects, i.e. *crosstalk* effects, between adjacent wires. Such effects include delay and noise injection and are a serious performance limitation in deep submicron VLSI circuits. An analytical model of the crosstalk effects would be extremely useful both in the design front-end and in the design back-end. For instance, a net ranking procedure based on such model could efficiently identify potential signal integrity problems between nets. A compact model of the coupled noise pulse amplitude which improves considerably the simple charge sharing model has been proposed in [4]. In our paper we will demonstrate that such model turns out to be quite inaccurate in several cases that often occur in practical circuits, because it does not consider the wire resistance. Moreover we will introduce an heuristic technique that allows to take into account the resistive effects, thus achieving a considerable accuracy improvement at an equivalent computational cost.

I - Introduction

Coupling effects between adjacent interconnect lines represent a serious limitation to performances and functionality of high speed electronic systems [1], [2], [3]. Therefore the verification of the crosstalk effects on signal integrity and delay, along with design techniques that minimize such effects by construction, are of the utmost importance in deep submicron VLSI circuit design. The availability of an efficient estimator of the impact of coupled noise on a given signal is a crucial element for crosstalk avoidance during the routing phase and for crosstalk aware timing verification techniques. Because of the huge number of interconnect lines in industrial VLSI designs, it is impractical to apply an accurate dynamic delay back-annotation including coupled noise on every net. Therefore a preliminary screening of the potentially crosstalk prone nets is needed. Usually this is done by using a simple charge sharing model, thus yielding the following equation for the coupled noise voltage amplitude [3]:

$$V_{xtalk} = V_{DD} \cdot \frac{C_C}{C_C + C_{GND}} \tag{1}$$

where C_C is the total lumped coupling capacitance between the victim and aggressor, C_{GND} is the total lumped capacitance to ground of the victim and V_{DD} is the switching aggressor voltage value (in all our examples $V_{DD} = 2.5V$). The expression in (1) does not take into account neither the signal driving strength nor the interconnect resistance, and therefore it may be considerably inaccurate. An improved model of the crosstalk voltage amplitude which includes the effects of the output impedance of the driving gates has been presented in [4]. A closed form expression for the peak amplitude of the coupled noise injected by one or more aggressors is derived under the assumption that the victim line is quiet. Since the noise pulse can be considered a small signal, linearity and time-invariance can be assumed.



R_1 driver resistance of the aggressor

C_1 total line capacitance of the aggressor

R_2 output resistance of the victim

C_2 total capacitance to ground of the victim

C_C coupling capacitance

Fig. 1:Equivalent circuit for the model proposed in [4]

Hence, the contribution of every aggressor, when all the other aggressors and the victim are grounded, can be analyzed separately and the total voltage noise peak can be obtained by superposition. The equivalent circuit used to derive the model in [4] is shown in Figure 1. By writing the nodal equations for the output node of the victim, an upper bound for the amplitude of the peak noise is obtained, thus yielding the following expression:

$$V_P = \frac{V_{DD}}{1 + \frac{C_2}{C_C} + \frac{R_1}{R_2}\left(1 + \frac{C_1}{C_C}\right)}. \tag{2}$$

When $\frac{R_1}{R_2} \to 0$ the expression in (2) reduces to $V_{DD} \cdot \frac{C_C}{C_C + C_2}$, which is similar to the charge sharing model (1). As it can be seen from Figure 1 and from expression (2), the model in [4] does not take into account the interconnect resistance. Therefore it neglects both the resistive shielding effect and the attenuation of the signal strength along the wire. In this paper we will show that neglecting these effects may lead to inaccurate predictions of the

relative sensitivity to coupled noise. Moreover we will present a simple heuristic, based on a dominant pole approximation, which takes into account the interconnect resistance. We will show that by applying this heuristic, a significant improvement of the predictive power of the model can be obtained with negligible additional computational cost. The accuracy of the improved model will be demonstrated on a large set of examples taken from real designs in a 0.25 μm, 6 metal layers, high-speed CMOS technology. The paper is structured as follows. The impact of interconnect resistance on the crosstalk effects is shown in Section II. The improved model of the coupled voltage noise amplitude is presented in Section III, and in Section IV experimental results on a set of realistic test cases are reported. Finally, in Section V some closing remarks are given.

II - Impact of wire resistance on coupled voltage noise amplitude

The interconnect delay represents a serious limitation to VLSI circuit performances in sub half-micron technologies [5]. In particular, wire resistance per unit length, being inversely proportional to the metal pitch, constantly increases with each new technology generation. Metal and via resistance have an impact on both gate and interconnect delay. The impact on gate delay is due to the resistance shielding effect, as illustrated in [6], which reduces the actual load seen by the gate with respect to the total capacitance to ground of interconnect and fan-out gates. Moreover the interconnect resistance, being in series with the equivalent output resistance of the gate, attenuates the strength of the driver and, as a consequence, the rise/fall time increases moving from drivers to loads [7], [9]. When considering coupled clusters of interconnects the effect of wire resistance is complicated by the fact that a given driver may interact with neighboring signals, thus acting either as a victim or as an aggressor. When acting as a victim, the resistance shielding effect contributes to increase the susceptibility of the given signal to coupling noise, because it decreases the actual capacitance to ground seen by the driver. On the other hand, the effect on the aggressor signals is to reduce their strength, thus decreasing the amplitude of the coupling noise injected on the neighboring wires. In order to quantify these effects we have designed the simple test case shown in Figure 2. It consists of two isomorphic circuits. The first circuit (Figure 2a) includes two segments of metal-4 running in parallel for 500μm at the minimum pitch in a 0.25μm minimum feature size, 6 metal layers CMOS technology (*SUBCKT_COUP*). The line terminates on an inverter driving a capacitive load. The victim driver is connected directly to one of the two coupled wires, whereas the aggressor signal is driven from a 4mm long line also routed in

metal-4 (*SUBCKT_WIRE*).

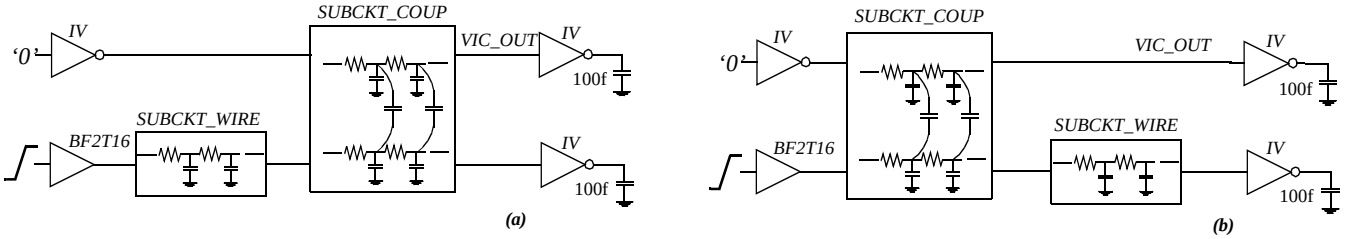


Fig. 2:Test-cases used to show the effect of wire resistance on a coupled RC network; *(a)* aggressor driver far off with respect to the coupled section; *(b)* aggressor driver near to the coupled section.

In the second circuit (Figure 2b) the same basic blocks have been combined in order to maintain the same total lumped capacitance to ground of each wire as in the first circuit. However the aggressor driver is connected directly to the coupled section of the network, and 4 mm of metal-4 are routed between the end of the coupled network and the aggressor load. The driving gates, IV and BF2T16, have been modeled by using a Thevenin equivalent circuit. The pre-characterized output resistance was respectively, 1.44 KΩ and 133Ω. The amplitude of the coupled noise was measured at the input of the victim receiver (*VIC_OUT*). The results of circuit simulations are reported in Figure 3.

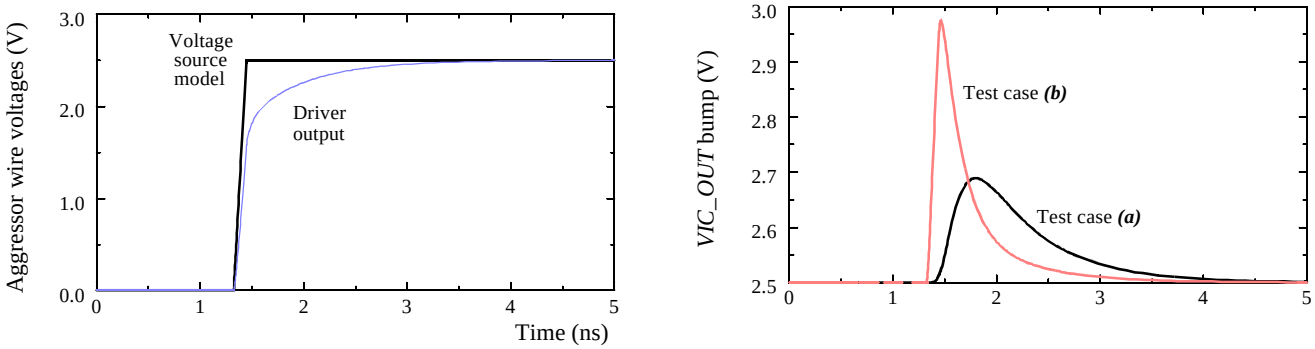


Fig. 3:Simulation waveforms for the test case shown in Figure 2.

We compared circuit simulation results with the predicted noise amplitude obtained by using the charge sharing model (1) and the model described in (2). It has to be noted that, by neglecting the resistance of the wires, the model parameters for both circuits are identical, namely:

R_1 = 133 Ω C_1 = 1.27 pF R_2 = 1441 Ω C_2 = 53.7 fF C_C = 49.4 fF

TABLE 1: COUPLED NOISE VOLTAGE AMPLITUDE MODEL COMPARISON.ALL UNITS ARE IN VOLTS.

	ELDO	Charge Sharing eq. (1)	Vittal/Marek-Sadowska Model: eq. (2)
Circuit (2a)	**0.189**	**1.198**	**0.549**
Circuit (2b)	**0.475**	**1.198**	**0.549**

The results are summarized in Table 1. It is possible to observe that the model in [4] is a much better approximation of the true value than the simple charge sharing model. However it is also evident that both models can not account for the reduced aggressor strength due to the extra wire resistance between the driver and the coupled network in circuit 2a. However the coupled noise amplitude in this case is less than half of that measured in circuit 2b. From the previous example, it seems evident that by exchanging the role of victim and aggressor, it is possible to generate a test case in which both equations (1) and (2) produce an optimistic estimation of the true coupled noise voltage amplitude. The circuit realization for this test case is shown in Figure 4.

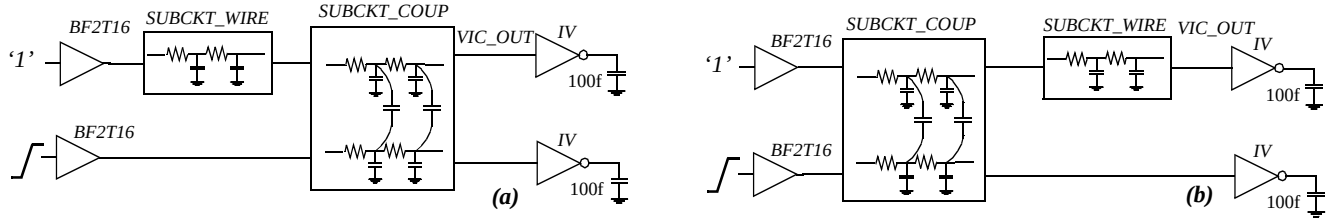


Fig. 4:Test-cases in which the equation (2) underestimate the true value of the coupled noise voltage amplitude; *(a)* Victim driver far with respect to the coupled section; *(b)* Victim driver near to the coupling section.

In order to account for the larger load due to the additional 4mm of interconnect, a buffer with a much greater driving strength is used to drive the victim signal. As a consequence the new value of the parameters used in (1) and (2) is:

$R_1 = 133.3\ \Omega \quad C_1 = 1.27\ \text{pF} \quad R_2 = 133.3\ \Omega \quad C_2 = 822\ \text{fF} \quad C_C = 49.4\ \text{fF}$

TABLE 2: COUPLED NOISE VOLTAGE AMPLITUDE MODEL COMPARISON. ALL UNITS ARE IN VOLT

	ELDO	Charge Sharing: eq. (1)	Vittal/Marek-Sadowska: eq. (2)
Circuit (4a)	**0.126**	**0.142**	**0.056**
Circuit (4b)	**0.035**	**0.142**	**0.056**

The results of circuit simulation and model evaluation for circuit 4a and 4b are summarized in Table 2. As expected, the resistance of the wire between the victim driver and the coupled section of interconnects attenuates the driving strength of the victim signal. Therefore the measured coupled noise amplitude in circuit 4a is more than 3 times larger than that in circuit 4b. Moreover it is important to note that, firstly the model described by (2) underestimates the actual noise voltage amplitude and secondly and more important, both methods yield identical values in the two cases (circuits 4a and 4b respectively), hence they cannot be used to sort circuit interconnects according to their relative susceptibility to crosstalk noise. In the next section we will show how it is possible to modify the model presented in [4] in order to take into account wire resistance.

III - Improved coupled noise amplitude model

In order to account for the dissipative component of the interconnects impedance, we propose to add a resistor R_E in series to the driver resistance R_1, as shown in Figure 5. Such resistor accounts for the reduced strength of the driver and also shields the actual capacitive load seen by the gate. In order to determine the value of R_E, we propose to use a single pole (dominant pole) approximation for the transfer function of the interconnect network representing the aggressor and victim lines. The dominant time constant of a linear, lumped time invariant RC tree can be approximated by using the popular delay metric known as the Elmore delay [8], defined by:

$$T_D = -m_1 = \int_0^\infty t h(t) dt \tag{3}$$

where $h(t)$ is the impulse response of the tree, and m_1 is its first moment. As shown in [9], m_1 can be related to the poles and zeros of the RC tree transfer function:

$$m_1 = b_1 - a_1$$
$$\text{with} \quad b_1 = \sum \frac{1}{p_i} \text{ and } \quad a_1 = \sum \frac{1}{z_i} \tag{4}$$

where p_i is the $i-th$ pole and z_i the corresponding zero. When no low-frequency zeros are present and one of the poles is dominant, i.e.:

$$\frac{1}{p_d} \ll \frac{1}{p_j}, \quad j = 1, \ldots, \text{no. of poles}, \; j \neq d$$

then:

$$T_D \cong -\frac{1}{p_d}. \tag{5}$$

Therefore in order to build a simple model of a complex RC tree we can use a single lumped RC low pass circuit characterized by the same time constant, i.e. such that $RC = T_D$. As the total capacitance to ground should be preserved, the value of R_E to be used in the model shown in Figure 5 is:

$$R_E = \frac{T_D(i)}{C_{TOT}} = \frac{\sum_j R_{ij} C_j}{C_{TOT}} \tag{6}$$

where C_{TOT} is the total lumped capacitance to ground of the RC tree, R_{ij} is the resistance of the path from the driver to node j that is common to the path from source to node i, and C_j is the capacitance to ground of node j. In our algorithm, node i represents the first node from the driver along a given path for which we want to estimate the effect of crosstalk, that presents a non-zero coupling capacitance to another node (e.g. the node *INT* in Figure 5). It is possible to show [8] that the Elmore delay can be computed in linear time with respect to the size of the RC tree, therefore the computation of R_E does not significantly increase the complexity of the algorithm with respect to the model presented in [4].

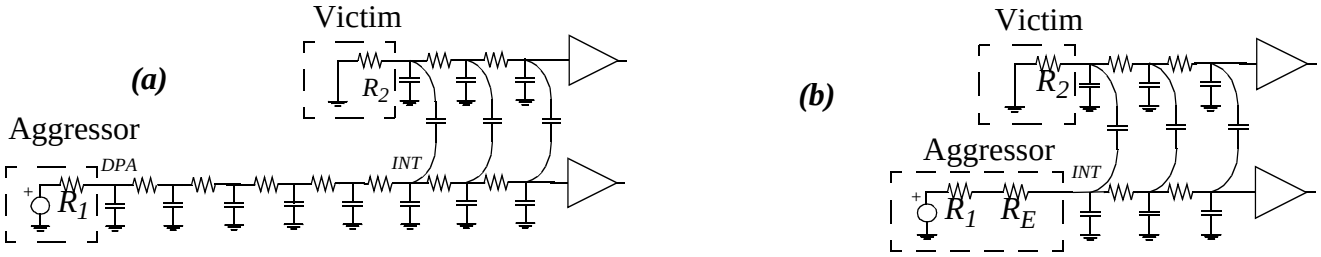


Fig. 5:Example of coupling occurring at the end of a resistive (aggressor) line *(a)* and proposed model *(b)*.

IV - Experimental Results

The proposed method has been used to rank all the interconnects of a large Layout Parasitic Extraction (LPE) data-base based according to their susceptibility to crosstalk noise. This data-base was obtained by using ARCADIA [11] on the layout of a general purpose, high performance DSP microprocessor, fabricated in a 0.25μm, 6 metal layers CMOS technology, and containing more than 6 millions of transistors (including memories) and several thousands of interconnects. After ranking and sorting all the nets according to decreasing order of coupled noise amplitude, the ones that turned out to be more affected by

crosstalk noise injection were further analyzed in detail by using the efficient crosstalk analysis tools described in [10], in order to verify both signal integrity and timing correctness of the circuit.

TABLE 3: COUPLED NOISE VOLTAGE AMPLITUDE COMPARISON. ALL UNITS ARE IN VOLTS.

	ELDO	Vittal/Marek Sadowska model	This Work
Circuit (2a)	**0.189**	**0.549 (190%)**	**0.221 (17%)**
Circuit (2b)	**0.475**	**0.549 (16%)**	**0.549 (16%)**
Circuit (4a)	**0.126**	**0.056 (-55%)**	**0.100 (-20%)**
Circuit (4b)	**0.035**	**0.056 (60%)**	**0.056 (60%)**
Test case #1	**0.464**	**0.756 (62%)**	**0.590 (27%)**
Test case #2	**0.089**	**0.160 (80%)**	**0.084 (-6%)**
Test case #3	**0.317**	**0.347 (9%)**	**0.347 (9%)**
Test case #4	**0.095**	**0.086 (-9%)**	**0.095 (0%)**

By analyzing some of the test cases extracted from the described experiment, it was possible to identify several real interconnect configurations for which the signal attenuation due to wire resistance contributed significantly to either decrease or increase the actual crosstalk noise amplitude. One of such test cases is shown in Figure 6. The results of the comparison between circuit simulations, the model described in (2) and our model, on some of the extracted test cases are summarized in Table 3. In all the test cases that have been analyzed, our model was significantly more accurate than the model presented in [4], with an average percentage error of 19% instead of 60%. The maximum percentage error that was observed on circuit 4b (~60%) actually corresponds to an absolute error of only 25 mV.

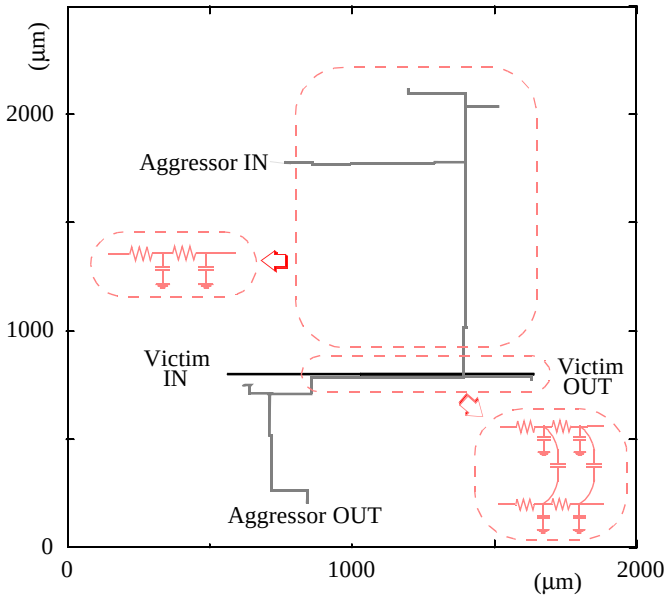


Fig. 6:Layout of the two nets of test-case #2

Moreover our model, by including the effect of wire resistance, allows to sharply discriminate the difference between the effect of coupling on circuits 2a, 4a and that on circuits 2b, 4b. In order to verify the capability of the model of detecting the impact of wire resistance on crosstalk effects, the relative difference of the coupled noise amplitude observed between circuits 2a, 4a and circuits 2b, 4b has been reported in Table 4.

TABLE 4: RELATIVE COUPLED NOISE VOLTAGE AMPLITUDE COMPARISON.

	ELDO	**Our model**
$(2b-2a)/(2a)$	**1.50**	**1.48 (1.3%)**
$(4b-4a)/(4a)$	**-0.72**	**-0.78 (8.3%)**

It is possible to observe that the relative variation of the noise amplitude predicted by our model is in excellent agreement with circuit simulation results, whereas both models in (1) and (2) cannot distinguish between the two different circuit configurations, thus predicting the same crosstalk noise value in both cases.

V - Conclusions

In this paper a technique for including the effect of wire resistance in a compact and efficient model of the crosstalk noise amplitude has been presented. It has been shown that, by neglecting the effect of wire resistance it is not possible to detect the different suscep-

tibility to crosstalk noise existing in several practical cases. Therefore not only our methodology achieves a much better accuracy, but also allows to perform an accurate ranking of the relative importance of crosstalk effects on different interconnects. The proposed technique has been applied to generate a ranking based on crosstalk noise susceptibility of the interconnects of a multi-million transistors circuit, fabricated in a deep submicron, state of the art CMOS technology. By comparing the results of model evaluations with circuit simulations on a set of interconnects taken from the layout of the previously described circuit, it was possible to demonstrate the excellent accuracy and resolution capabilities of the proposed method.

VI - References

[1] H. Sasaki, “Multimedia: Future and Impact for Semiconductor Technology”, in Proc. of International Electron Devices Meeting, 1997, pp. 3-8

[2] X. Zhang, “Coupling Effects on Wire Delay”, IEEE Circuits & Devices Magazine, pp. 12-18, Nov. 1996

[3] L. Gal, “On-chip Crosstalk-the New Signal Integrity Challenge”, in Proc. Custom Integrated Circuits Conference, 1995, pp. 251-254

[4] A. Vittal and M. Marek-Sadowska, “Crosstalk Reduction for VLSI”, IEEE Transaction on CAD, Vol. 16, No. 3, pp. 290-298, March 1997.

[5] M. T. Bohr, “Interconnect Scaling - The Real Limiter to High Performance ULSI”, in Proc. of International Electron Devices Meeting, 1995, pp. 241-244

[6] J. Quian, S. Pullela and L.T. Pileggi, “Modeling the Effective Capacitance for the RC Interconnect of CMOS Gates”, IEEE Trans. on CAD, vol 13 (12), Dec. 1994, pp-1526-1535

[7] E.G. Friedman and J.H. Mulligan Jr. “Ramp Input Response of RC Tree Networks”, in Proc. IEEE ASIC Conference, 1996, pp. 63-66

[8] P. Penfield and J. Rubinstein “Signal Delay in RC Tree Networks”, in Proc. of the 19th Design Automation Conference, 1981

[9] R. Gupta, B. Krauter, B. Tutuianu, J. Willis and L.T. Pileggi, “The Elmore Delay as a Bound for RC Trees with Generalized Input Signals”, in Proc. IEEE/ACM Design Automation Conference, 1995, pp. 364-369

[10]D. Pandini, P. Scandolara and C. Guardiani, “Reduced Order Macromodel of Coupled Interconnects for Timing and Functional Verification of Sub Half-micron IC Designs”, In Proc. Asia and South Pacific Design Automation Conference, 1998, pp. 45-50

[11]S. Napper, “Technical White Paper on RC Extraction” Technical report, EPIC Design Technology, Inc., 1995