Accurate Junction Capacitance Modeling for Substrate Crosstalk Calculation

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1. Abstract

This paper presents a modeling technique to be used in substrate coupling computation of mixed-signal circuits. Substrate crosstalk can negatively impact the performance of analog circuit elements such as mixers or amplifiers and can lead to a total breakdown of circuit parts. In order to forecast substrate-related problems and to analyze its influence EDA-tools are needed that can be applied during layout verification. Depending on the degree of accuracy interfaces between the designed elements and the substrate region have to be modeled. A very important issue is the calculation of junction capacitors. We propose a method that is capable of accurately determining lumped junction capacitors without measurement or device simulation.

2. Introduction

Since distances between components decrease as well as their size and as operating frequencies rise, crosstalk between components becomes increasingly important. Critical components are influenced not only by interconnect parasitics (resistivity of wires, capacitance to substrate and other wires) but also via substrate coupling. To avoid expensive redesigns of chip layout due to parasitic effects it is desirable to simulate and forecast malfunctional behavior before silicon is produced. An EDA-tool is needed that helps designers to avoid substrate-related coupling problems within the design loop. Recently, several approaches have been published [1-7] that help verifying the layout with respect

to the underlying substrate and its physical properties. Some of those approaches work with a 2,5-dimensional discretization of the substrate, others apply boundary element methods to a conducting semiplane. All of them derive a network description using lumped elements to represent the substrate region. The problem ahead is to accurately connect the substrate network to the network of the designed elements.

In CMOS circuits, for instance, capacitors model the depletion capacitance from the wells to substrate. It is necessary to divide the overall capacitance into smaller fractions. Fig. 1 shows an example of an arbitrarily shaped well and a possible arrangement of capacitors.

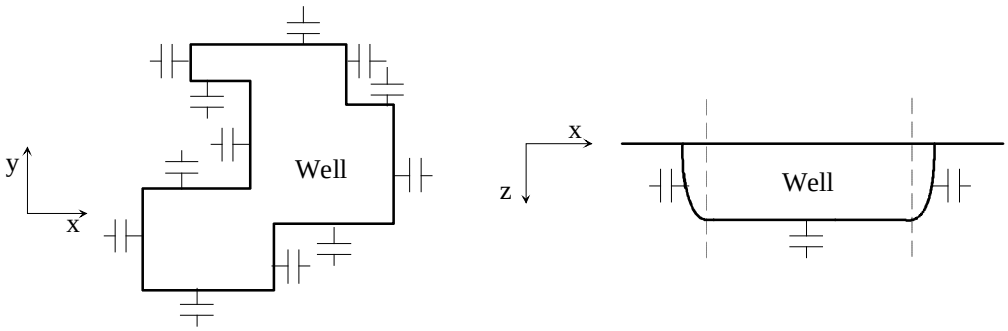

Fig. 1: Capacitor fractions of a well

Fig. 2 shows a fragment of a sidewall and the surfaces of the discretization. Each surface of the sidewall represents the area of a partial junction capacitor.

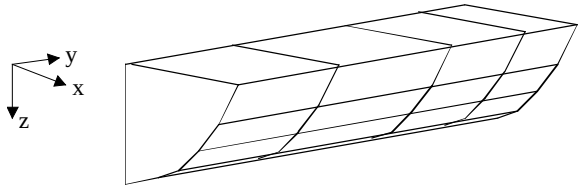

Fig. 2: Sidewall discretization

Normally a plate capacitor model is used to determine the value of each capacitor. As we found out (see results) this assumption holds for the bottom of the well but does not hold for the sidewalls.

3. Basic Formulas

The well depletion-layer capacitor is determined under the assumptions that

- the electric field outside the space-charge region equals zero,
- the overall charge of the space-charge region equals zero,
- the electric field is continual,
- the doping concentration changes abruptly at the junction.

Under these circumstances the width of the space-charge region is

$$l_s = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{q}(U_D - U)\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \tag{1}$$

with q being the electrical charge, N_A and N_D the mean impurity concentrations on opposite sides of the junction, U_D the diffusion voltage and U the actual voltage drop between the two sides. The profile is assumed to be Gaussian so that in the vicinity of the junction the doping concentration is given by

$$N(z') = N_B \cdot \left[\exp\left(-\frac{z'}{\lambda}\right) - 1\right] \tag{2}$$

with

$$\lambda = \frac{L_D}{\ln\frac{N_0}{N_B}} \tag{3}$$

N_B stands for the substrate doping concentration, L_D is the diffusion length, N_0 denotes the surface concentration. The usual way to determine a fraction of the overall capacitance is to assume a plate capacitor and calculate the capacitance as

$$C = \frac{\varepsilon_0\varepsilon_r A}{l_s} \tag{4}$$

where A is the appropriate face area for a part of the well (side or bottom). The comparison between simulation and results (see below) shows that in this way the sidewall capacitors are highly underestimated. Therefore, we propose to use the cylindrical capacitor model and the spherical capacitor model, respectively. Their capacitances are determined as

$$C_{cyl} = \frac{2\pi l \varepsilon_0 \varepsilon_r}{\ln\left(\frac{r_2}{r_1}\right)} \quad . \tag{5}$$

with r_1 denoting the inner and r_2 the outer radius and l the length of the cylindrical capacitor;

$$C_{sph} = \frac{4\pi\varepsilon_0\varepsilon_r r_1 r_2}{r_2 - r_1} \tag{6}$$

with r_1 being the inner and r_2 the outer radius of the spherical capacitor. It can be seen from Fig. 1 and Fig. 3 that three different regions exist:

1. a planar region for the bottom
2. a cylindric region for the sidewalls
3. a spheric region for the corners

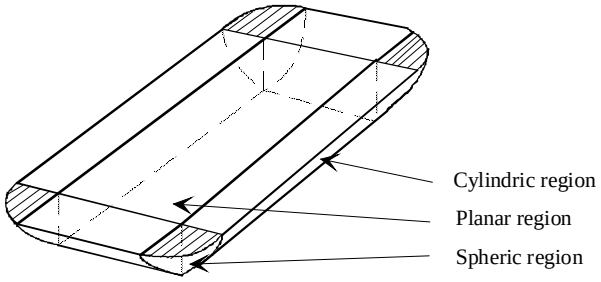

Fig. 3: Different regions

4. Sidewall calculation

Due to the lateral diffusion length *o*, with *o≠d* the shape of the sidewalls is elliptical instead of cylindrical.

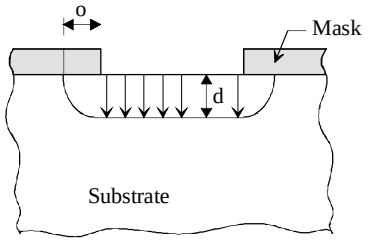

Fig. 4: Diffused region

Fig. 5 shows a cut through a sidewall. F1 through F5 are five surfaces that result in five junction capacitors, that may be combined later on. First the height *h* and the width *w* are determined for each surface. To do so, the range of the quarter-ellipse is divided into equal parts depending on the maximal structure size. The

equation for the ellipse (7) and the equation for the cutting line (8) lead to the points necessary for the determination of the surfaces.

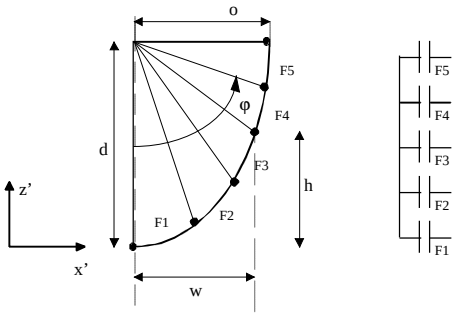

Fig. 5: Cut through a sidewall

$$\frac{x'}{o^2}+\frac{(z'-d)^2}{d^2}=1 \tag{7}$$

$$\frac{x}{d\cdot\tan\left(\frac{\pi}{2}\cdot\frac{level}{n\_lev}\right)}+\frac{z'}{d}=1 \tag{8}$$

Level stands for the actual level and *n_lev* for the number of levels (in Fig. 4 level=5). Solving the equations for *x'* and *z'* leads to the desired intersection points. This way *h* and *w* for the upper and for the lower point and the center of gravity can then be determined. With the doping concentrations of the center of gravity (Fig. 6) the junction capacitor C_F for the surface fraction *F* is determined using the mean radius r_m

$$r_m=\sqrt{r_A * r_B} \tag{9}$$

$$C_F=\frac{\varepsilon_0\varepsilon_r l|\varphi_A-\varphi_B|}{\ln\left(\frac{r_m+l_s}{r_m}\right)} \tag{10}$$

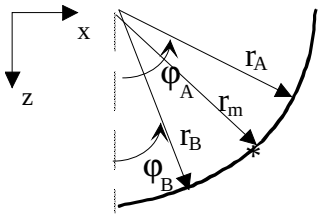

Fig. 6: Approximating the elliptic shape

5. Corner calculation

At the corners a spherical approach applies (Fig. 3a). As the corners always have the surface of one eighth of the surface of a sphere, we can calculate the capacitance of one corner as

$$C_{corner} = \frac{1}{8} \cdot \frac{4\pi\varepsilon(r_m + l_s)r_m}{l_s} \tag{11}$$

If the surface is divided into smaller fractions it is possible to divide the corner capacitor into smaller fractions, according to the area of the surface fractions related to the surface of the whole corner.

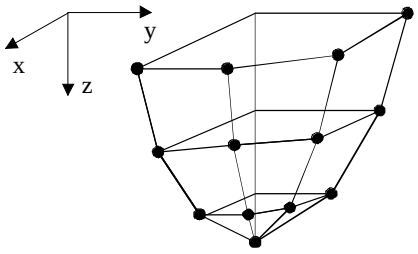

Fig. 7: Corner of a well

6. Experimental Results

The algorithm has been applied to the calculation of a junction capacitor C_{j0} with voltage U=0V. We used the algorithm with three examples. Common to all of them is a p-doped layer within an n-doped epitaxial layer. The implantation layer areas are depicted in Fig. 8.

Fig. 8 shows two filled areas and one ring-shaped area. D1 and D2 represent two different processes. The concentration of the epitaxial layer N_B, the position of the pn-junction x_j and the surface-concentration N_0 can be extracted from doping profiles and are given in Tab. 1.

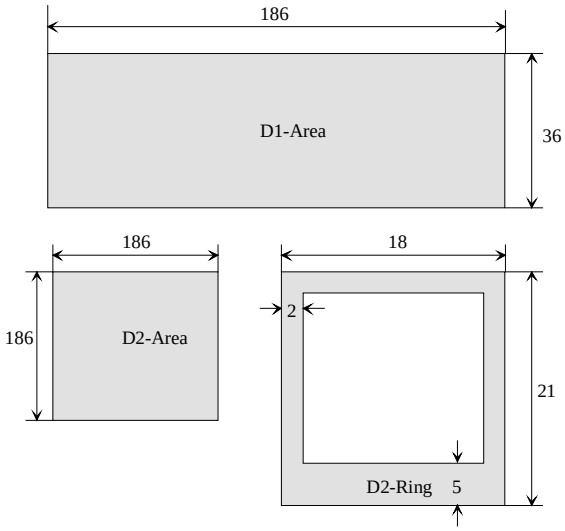

Fig. 8: Examples (all measures in μm)

	N_B [cm^{-3}]	x_j [μm]	N_0 [cm^{-3}]
D1	3.3E+15	0.56	3.8E+18
D2	3.3E+15	0.74	2.5E+19

Tab. 1: Physical properties of processes

In order to compare measured and calculated results it is necessary to divide the measured pn-junction capacitors into sidewall and bottom fractions. Therefore, equation (12) has to be applied to the measured results.

$$C_{j0} = A \cdot area + B \cdot periphery \tag{12}$$

In order to get factors A and B a bunch of C(V)-measurements are performed with different geometries with varying periphery-to-area ratios. Taking into account all the 0V-values it is possible to separate the two parts using an easy fitting.

The following table and diagrams show comparisons between measured and simulated values. “Old way” is an algorithm working on the same discretization as “New Way”, however, all surface capacitors are calculated with the plate-capacitor model. The table and the diagram also show three columns for each approach and the measurements, respectively. One is for the bottom part, one for the whole sidewall part and one for the overall junction capacitor. Tab. 2

demonstrates the results for the examples called “D1-Area”, “D2-Area” and “D2-Ring” (see Fig. 8).

D1-Area	Bottom [pF]	Sides [pF]	Total [pF]
Old way	1,2036	0,0744	1,2780
New way	1,2021	0,1461	1,3482
Measured	1,1800	0,1540	1,3340

D2-Area	Bottom [pF]	Sides [pF]	Total [pF]
Old way	6,5903	0,1608	6,7511
New way	6,5904	0,2327	6,8231
Measured	6,6400	0,2450	6,8850

D2-Ring	Bottom [pF]	Sides [pF]	Total [pF]
Old way	0,0339	0,0286	0,0625
New way	0,0341	0,0421	0,0762
Measured	0,0349	0,0441	0,0790

Tab. 2: Comparisons for example “D1-Area, D2-Area, D2-Ring”

As to be seen in Tab. 2 the main part of the total junction capacitor is formed by the bottom portion for D1-Area and D2-Area. In the case of D2-Ring the sidewall part is even larger than the portion of the bottom part. The calculation with the plate-capacitor-method leads to results which are much too small compared to the measured values.

To emphasize the main differences Fig. 9, 10 and 11 show the relative error with the measured values as a reference. For the sidewall capacitors the deviation lies between 30% and 50% for the old method and under 5% for the new approach. The total capacitor of the ring structure was determined with a deviation of about 20% with the old method and a deviation of about 5% with the new method.

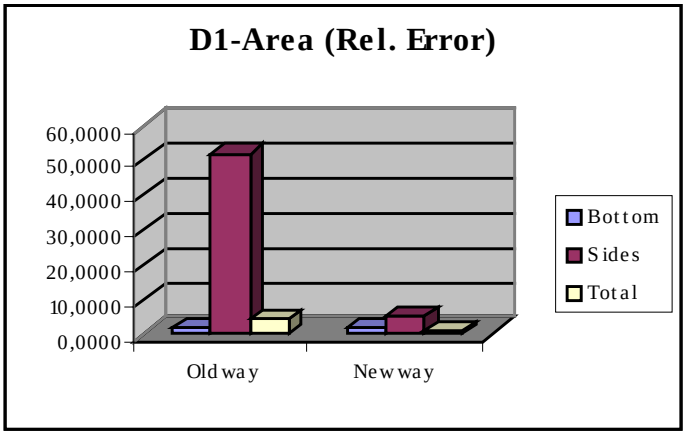

Fig. 9: Relative Error for D1-Area

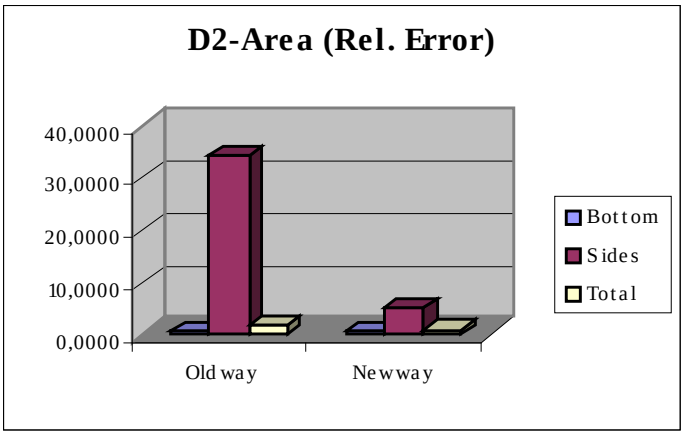

Fig. 10: Relative Error for D2-Area

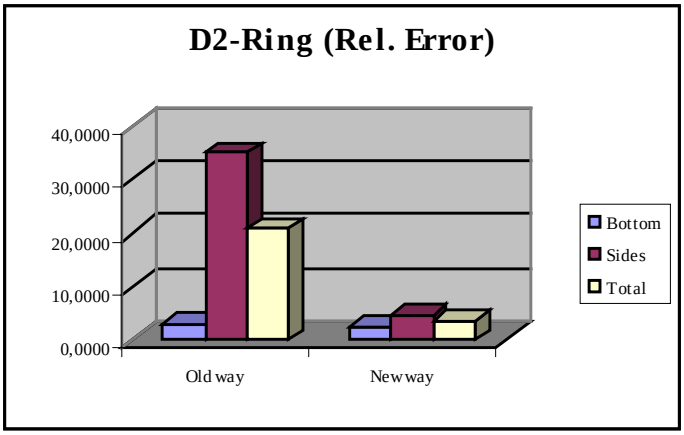

Fig. 11: Relative Error for D2-Ring

7. Conclusions

Substrate coupling problems are a challenge for mixed-signal circuit designs. It is necessary to foresee possible problems and to analyze the circuit behavior before silicon is processed. Therefore, EDA-tools are needed that try to map physical properties into circuit elements. An important issue is the calculation of junction capacitors connecting circuit elements to the substrate. In this paper we presented a procedure to accurately determine junction capacitors without the necessity of device-level simulations or measurements.

8. Acknowledgement

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9. References

[1] Wemple, I., Yang, A.T., *Integrated Circuit Substrate Coupling Models Based on Voronoi Tessellation*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 14, N°12, Dec. 1995, pp. 1459-1468

[2] Verghese, N.K., Allstot, D.J., *Computer Aided Design Considerations for Mixed-Signal Coupling in RF Integrated Circuits*, IEEE Journal of Solid-State Circuits, Vol. 33, N°. 3, Mar. 1998, pp. 314-323

[3] Smedes, T., van der Meijs, N.P., van Genderen, A.J., *Extraction of Circuit Models for Substrate Crosstalk*, Proceedings of Design Automation Conference 1995, pp. 199-206

[4] Gharpurey, R., Meyer, R.G., *Modeling and Analysis of Substrate Coupling in Integrated Circuits*, IEEE Journal of Solid State Circuits, Vol. 31, pp. 344-353, Mar. 1996

[5] Clement, F.J.R.., Zysman, E., Kayal, M., Declercq, M., *Layout Inspection Tool Dedicated to the Parasitic Coupling Effects through the substrate of Integrated Circuits*, Proceedings of PATMOS 1995, pp. 267-276

[6] Stanisic, B.R., Verghese, N.K., Rutenbar, R., Carley, L.R., Allstot, D.J., *Adressing Substrate Coupling in Mixed Mode ICs: Simulation and Power Distribution Synthesis*, IEEE Jounal of Solid-State Circuits, Vol. 29, N° 3, 1994, pp. 226-238

[7] Hegedus, S.S., *Parasitic Isolation PNP Devices and Their Effect on NPN Saturation Delay*, Design Automation Conference 1980, pp. 107-111