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THE ADVANCE PROGRAM AT A GLANCE

19.30 - 21.00 Welcome Cocktail and Registration	07.00 - 21.00 Social Activities, Excursions: see page 9	Sunday, August 27	Monday, August 28
19:30 Banquet at the Parkhotel	16:05 - 16:30 Coffee Break 16:30 - 18:35: Technology Mapping and R & P	19:30 Boat Trip on Lake Ossiach with dinner	9:00 - 10:30 Plenum Session 1
			10:30 - 11:00 Coffee Break 11:00 - 12:40: Network Processors Prototyping
19:30 Boat Trip on Lake Ossiach with dinner	16:05 - 16:30 Coffee Break 16:30 - 18:35: Biologically Inspired Methods	19:30 Boat Trip on Lake Ossiach with dinner	8:30 - 10:30 Plenum Session 2
			10:30 - 11:00 Coffee Break 11:00 - 12:40: Mobile Communication
19:30 Boat Trip on Lake Ossiach with dinner	16:05 - 16:30 Coffee Break 16:30 - 18:35: Applications 1 Optimization	19:30 Boat Trip on Lake Ossiach with dinner	8:30 - 10:30 Plenum Session 3
			10:30 - 11:00 Coffee Break 11:00 - 12:40: Architectures and Technology
19:30 Boat Trip on Lake Ossiach with dinner	16:05 - 16:30 Coffee Break 16:30 - 18:35: Applications 2 Optimization	19:30 Boat Trip on Lake Ossiach with dinner	14:00 - 15:40: Compilation and Related Issues
			12:40 - 14:00 Lunch Break 14:00 - 15:40: Applications 2
19:30 Boat Trip on Lake Ossiach with dinner	16:05 - 16:30 Coffee Break 16:30 - 18:35: Applications 1 Optimization	19:30 Boat Trip on Lake Ossiach with dinner	14:00 - 15:40: Compilation and Related Issues
			12:40 - 14:00 Lunch Break 14:00 - 15:40: Applications 2
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			12:40 - 14:00 Lunch Break 14:00 - 15:40: Applications 2
19:30 Boat Trip on Lake Ossiach with dinner	16:05 - 16:30 Coffee Break 16:30 - 18:35: Applications 1 Optimization	19:30 Boat Trip on Lake Ossiach with dinner	14:00 - 15:40: Compilation and Related Issues
			12:40 - 14:00 Lunch Break 14:00 - 15:40: Applications 2

EARLY REGISTRATION DEADLINE:
JULY 30
YOU SAVE 35 EURO

GENERAL CHAIR:

Herbert Grünbacher
 Carinthia Tech Institute
 Richard-Wagner-Strasse 19
 A-9500 Villach
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PROGRAM CHAIR:

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 Germany
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PLACE

VILLACH AND CARINTHIA

Carinthia is the southernmost province of Austria. It extends 9,533 km² to the south of the main alpine ridge and borders on Slovenia and Italy. 56 % of the state lies above an altitude of 1,000 m, the climate is characterised by the Mediterranean influence.

For a good **2,000 years**, the most direct route from the north to the south of Europe has led through the present-day Carinthia. Where the Roman legions once marched, the Tauern motorway today connects Hamburg with Palermo. It takes 3 hours from Munich to Villach and not much longer to the important Mediterranean ports of Trieste and Genova or the capital of Austria, Vienna.

1,270 lakes, ice-covered peaks, the largest glacier of the Eastern Alps, roaring waterfalls, idyllic alpine pastures and of course, the Großglockner characterise the countryside of Carinthia.

Villach is a charming old town with Mediterranean flair, surrounded by a vacation area with clear bathing lakes, traditional thermal baths and numerous summer and winter sport resorts it is the ideal backdrop for a successful event.

Whether you relax on the Drau river after a hard days conference or go shopping in the old city centre or just head for your hotel - everything is right on the doorstep. Hot spring water swimming pools with their health-giving tradition, crystal clear lakes to swim in and hiking in the mountains are just some of the attractive features of this popular holiday region. Take advantage of them on a day out or bring the family with you for a short break.

(continued on page 29)



WEDNESDAY, AUGUST 30 AFTERNOON

14:00 - 15:40 APPLICATIONS 2

Chair: Toshiaki Miyazaki, NTT Laboratories

S. Ichikawa, H. Saito, L. Udorn, K. Konishi, Toyohashi U
Evaluation of Accelerator Designs for Subgraph Isomorphism Problem 14.00 - 14.25

M. Edwards, P. Green, UMIST
The Implementation of Synchronous Dataflow Graphs Using Reconfigurable Hardware 14.25 - 14.50

T. Courtney, R. Turner, R. Woods, The Queen's U Belfast
Multiplexer Based Reconfiguration for Virtex Multipliers 14.50 - 15.15

C. Bobda, T. Lehmann, U Paderborn
Efficient Building of Word Recognizer in FPGAs for Term-Document Matrices Construction 15.15 - 15.40

15.40 - 16.00 (CLOSING SESSION)

(continued from page 4)

SILICON ALPS:

TO WORK WHERE OTHERS GO FOR VACATIONS



Carinthia is known as a holiday resort, but it has more to offer than mountains, lakes and innumerable leisure-time opportunities. In fact only 10% of Carinthia's affluence is obtained from tourism. Industry is three times as strong and therefore the most important economic factor. Approximately 350 manufacturing companies employ a work force of around 28,000 people. The city of Villach, nestled in the Austrian Alps in Carinthia where Austria, Italy and Slovenia meet, is home to world class high technology companies like Infineon and SEZ, research centres like Carinthia Tech Research and quality educational institutions like the Carinthia Tech Institute, School of Electronics. In recent years the city has taken decisive and innovative steps to further grow its technology base by pursuing an economic development policy designed to create new jobs in the electronics and microelectronics sectors.

(continued on page 27)

(continued on page 27)

PROGRAM COMMITTEE:

Nazeeh Aranki, Jet Propulsion Laboratory, USA
Peter Athanas, Virginia Tech, USA
Samary Baranov, Ben Gurion University Negev, Israel
Jürgen Becker, Darmstadt University of Technology, Germany
Neil Bergman, Queensland University of Technology, Australia
Eduardo Boemo Scalvinoni, University of Madrid, Spain
Gordon Brebner, University of Edinburgh, Scotland
Klaus Buchenrieder, Infineon Technologies AG, Germany
Michael Butts, Synopsys, Inc., USA
Stephen Casselman, Virtual Computer Corp., USA
Bernard Courtois, TIMA Laboratory, France
Andre DeHon, California Institute of Technology, USA
Carl Ebeling, University of Washington, USA
Hossam Elgindy, University of Newcastle, Australia
Norbert Fristacky, Slovak Technical University, Slovakia
John Gray, Algotronix Ltd., UK
Manfred Glesner, Darmstadt University of Technology, Germany
Herbert Grünbacher, Carinthia Tech Institute, Austria
Stephen Guccione, Xilinx Inc., USA
Richard Hagelauer, Kepler-University of Linz, Austria
Wolfgang Halang, University of Hagen, Germany
Reiner Hartenstein, University of Kaiserslautern, Germany
Scott Hauck, University of Washington, USA
Michael Herz, University of Kaiserslautern, Germany
Thomas Hoffmann, University of Kaiserslautern, Germany
Brad Hutchings, Brigham Young University, USA
Udo Keschull, University of Leipzig, Germany
Andres Keevallik, Tallinn Technical University, Estonia
Andreas Koch, TU Braunschweig, Germany
Tom Kean, Algotronix Ltd., UK
Dominique Lavenier, Los Alamos National Laboratory, USA
Jason Lohn, NASA Ames Research Center, USA
Wayne Luk, Imperial College, UK
Patrick Lysaght, Strathclyde University, Scotland
Reinhard Männer, University of Mannheim, Germany
Bill Mangione-Smith, University of California at Los Angeles, USA
John McCanny, The Queen's University of Belfast, Northern Ireland
George Milne, University of South Australia, Australia
Toshiaki Miyazaki, NTT Laboratories, Japan
Ulrich Nageldinger, University of Kaiserslautern, Germany
Viktor Prasanna, University of Southern California, USA
Jonathan Rose, University of Toronto, Canada
Zoran Salcic, University of Auckland, New Zealand
John Schewel, Virtual Computer Corp., USA
Hartmut Schmeck, University of Karlsruhe, Germany
Christian Siemers, University of Applied Sciences Heide, Germany
Moshe Sipper, Swiss Federal Institute of Technology, Switzerland

The New Case for Reconfigurables: skyrocketing design cost and shrinking time to market are the case to switch from hardwired to reconfigurable IPs. Integration density of reconfigurable circuits is growing faster than that of hardwired logic. So the 2nd Design Crisis creates new opportunities and necessities for reconfigurable IP usage.

Products shipped incompletely specified, can be completed at customer's site by configuration code transmission over the internet for bug fixes, field upgrades, or, for customization, driven by interaction: don't miss the Wednesday keynote!

10:30 - 11:00 COFFEE BREAK**11:00 - 12:40 METHODOLOGY AND TECHNOLOGY**
Chair: Hartmut Schmeck, U Karlsruhe

- G.Constantinides, P.Cheung, W.Luk, IC London
Multiple-Wordlength Resource Binding 11.00 - 11.25
- M.Vasilko, G.Benyon-Tinker, Bournemouth U
Automatic Temporal Floorplanning with Guaranteed Solution Feasibility 11.25 - 11.50
- K.Aoyama, H.Sawada, A.Nagoya, K.Nakajima, NTT Laboratories
A Threshold Logic-based Reconfigurable Element with a New Programming Technology 11.50 - 12.15
- A.Krasniewski, Warsaw U
Exploiting Reconfigurability for Effective Detection of Delay Faults in LUT-Based FPGAs 12.15 - 12.40

12:40 - 14:00 LUNCH BREAK

(continued from page 29)

A major component of this policy is the Micro-Electronic Cluster, a network of technology companies focused on micro-electronics as well as their natural partners (suppliers, scientific and educational institutions, and government) that offer complimentary inputs.

REVIEWERS / COMMITTEES

Wolfgang Rosenstiel, University of Tübingen, Germany
Eduardo Sanchez, EPFL, Lausanne, Switzerland
Alexander Sedlmeier, Infineon Technologies AG, Germany
Micaela Serra, University of Victoria, Canada
Dimitrios Soudris, Democritus University of Thrace, Greece
Joern Stohmann, Infineon Technologies AG, Germany
Toshinori Sueyoshi, Kumamoto University, Japan
Russell Tessier, University of Massachusetts, USA
Anne-Marie Trullemans-Ankaert, Université catholique de Louvain, Belgium
Klaus Waldschmidt, University of Frankfurt, Germany
Norbert Wehn, University of Kaiserslautern, Germany
Markus Weinhardt, Imperial College, UK

STEERING COMMITTEE:

Manfred Glesner, Darmstadt University of Technology
John Gray, Algotronix Ltd., UK (lifetime honorary member)
Herbert Grünbacher, Carinthia Tech Institute, Austria
Reiner Hartenstein, University of Kaiserslautern, Germany
Andres Keevallik, University of Tallinn, Estonia
Wayne Luk, Imperial College, UK
Patrick Lysaght, Strathclyde University, Scotland

INDUSTRIAL LIAISONS:

Axel Sikora, BA Lörrach, Germany

MICHAL SERVIT AWARD COMMITTEE:

Gordon Brebner, University of Edinburgh, Scotland
Manfred Glesner, Darmstadt University of Technology, Germany
John Schewel, Virtual Computer Corp., USA (Sponsor)
Hartmut Schmeck, University of Karlsruhe, Germany
Hirotō Yasuura, Kyushu University, Japan

STUDENT PAPERS:

Peter Zipf, University of Siegen, Germany
Thomas Hoffmann, University of Kaiserslautern, Germany

PROCEEDINGS



The conference proceedings are published by Springer Verlag Berlin /Heidelberg /New York within the Lectures Notes on Computer Science (LNCS) Series (see: <http://www.springer.de/comp/lncs/>). The volume will be handed out to participants at check-in as part of the conference package.

TUESDAY - SOCIAL PROGRAM / DINNER

19:30 BOAT TRIP ON LAKE OSSIACH WITH DINNER

Lunches and social activities with dinner are included in the conference fee (except student rate). Details t.b.a. at Conference Site.

INDUSTRIAL EXHIBIT FACILITIES

Spaces available for exhibitors are inviting, and communicative, located in the center of the conference activities: attractive locations in a central wide and bright area located between lecture halls, where also the coffee breaks and the poster presentations will be located. Tables and chairs will be provided. Internet upon request. Also see pg. 11.

Registration is still open for exhibitors. Deadline is July 30. Exhibitor Registration Form on pages 15-18.

RETURN FLIGHTS FROM VILLACH

NON-STOP FLIGHTS FROM KLAGENFURT AIRPORT

SUMMER 2000 - DEPARTURES 27-05-00 - 28-10-00					
Changes without notice! - Warranty Disclaimer! - Check: http://www.klagenfurt-airport.at/english/linienfluege.htm					
Destination	Flight	Departure	Arrival	Days	
Frankfurt	FRA V0483	06.20	08.05	1	2 3 4 5 6 7
	V0485	13.30	15.20	1	2 3 4 5 6 7
	V0488	18.25	20.10	1	2 3 4 5 6 7
München (Munich)	MUC KL3200	08.00	09.00	1	2 3 4 5 - 7
	KL3202	17.20	18.20	1	2 3 4 5 - 7
Wien (Vienna)	VIE V0551/OS95	06.00	06.50	1	2 3 4 5 - -
	V0563/OS963	06.35	07.30	1	2 3 4 5 6 -
	V0553/OS953	08.40	09.30	1	2 3 4 5 6 7
	V0555/OS955	11.55	12.45	1	2 3 4 5 6 7
	V0557/OS957	15.15	16.25	1	2 3 4 5 - -
	V0559/OS959	18.20	19.10	1	2 3 4 5 6 7
Zürich	ZRH LX427	18.30	20.05	1	2 3 4 5 - 7
	LX325	13.05	14.35	-	- - - - 6 -

More Flights: Amsterdam, Hamburg, Köln (Cologne), Linz, Salzburg

for Arrivals see page 19. A conference shuttle service from Villach will be provided on Wednesday afternoon.

**MONDAY, AUGUST 28
MORNING**

**TUESDAY, AUGUST 29
AFTERNOON**

8:00 REGISTRATION OPENS

9:00 - 10:30 PLENUM SESSION 1
Chair: Herbert Grünbacher, Reiner Hartenstein

9:00 Welcome and Opening

9:15 Keynote: Tsugio Makimoto, Hitachi, Tokyo
The Rising Wave of Field-Programmability

10:00 Sriram Govindarajan, Ranga Vemuri,
U Cincinnati
*Tightly Integrated Design Space Exploration with
Spatial and Temporal Partitioning in SPARCS*

10:30 - 11:00 COFFEE BREAK

11:00 - 12:40 NETWORK PROCESSORS
Chair: Ton Kean, Algotronix, Inc.

J.Ditmar, K.Torkelsson, A.Jantsch, Ericsson: 11.00 - 11.25
*A Dynamically Reconfigurable FPGA-based Content
Addressable Memory for Internet Protocol
Characterization*

X.Tang, M.Aalsma, R.Jou, Chameleon Systems, Inc. 11.25 - 11.50
*A Compiler Directed Approach to Hiding
Configuration Loading Latency in
Chameleon Reconfigurable Chips*

M.Iliopoulos, T.Antonakopoulos, U Patras 11.50 - 12.15
*Reconfigurable Network Processors based on Field
Programmable System Level Integrated Circuits*

H.Fallside, M.Smith, Xilinx, Inc. 12.15 - 12.40
Internet Connected FPL

12:40 - 14:00 LUNCH BREAK



(See page 29.)
Are you interested in a
list of high tech firms?
You like to visit one of
them? Please, mailto:
hartenst@rhrk.uni-kl.de

14:00 - 16:05 STUDENT PAPERS 2

Chair: Th. Hoffmann, U Kaiserslautern

S.Wadhwa, A.Dandalis, USC 14.00 - 14.25
*Efficient Self-Reconfigurable Implementations
Using On-Chip Memory*

A.Glasmacher, K.Woska, U Siegen 14.25 - 14.50
*Design and Implementation of a XC6216 FPGA
Model in Verilog*

J.Andrejas, A.Trost, U Ljubljana 14.50 - 15.15
Reusable DSP Functions in FPGAs

M.Redekopp, A. Dandalis, USC LA 15.15 - 15.40
A Parallel Pipelined SAT Solver for FPGA's

A.Touhafi, U Brussel 15.40 - 16.05
*A Multi-Node Dynamic Reconfigurable Computing
System with Distributed Reconfiguration Control*

16:05 - 16:30 COFFEE BREAK

16:30 - 18:35 OPTIMIZATION
Chair: Rainer Spallek, U of Dresden

R.Enzler, T.Jeger, D.Cottet, G.Tröster, ETH Zürich 16.30 - 16.55
*High Level Area and Performance Estimation of
Hardware Building Blocks on FPGAs*

R.Tessier, H.Giza, U Massachusetts 16.55 - 17.20
Balancing Logic Utilization and Area Efficiency in FPGAs

J.Emmert, J.Cheatham, P.Kataria, C.Stroud, M.Abramovici,
U Kentucky, A.M.Taylor 17.20 - 17.45
*Performance Penalty for Fault Tolerance in Roving
aSTARs*

J.Qiao, M.Ikeda, K.Asada, U Tokyo 17.45 - 18.10
*Optimum Functional Decomposition for LUT-based
FPGA Synthesis*

M.Eisenring, M.Platzner, ETH Zürich 18.10 - 18.35
Optimization of Run-time Reconfigurable Embedded Systems

18:35 - 19:30 BREAK

19:30 BOAT TRIP, see page 25

**MONDAY, AUGUST 28
AFTERNOON**

**TUESDAY, AUGUST 29
MORNING**

14:00 - 16:05 DYNAMICALLY RECONFIGURABLE 1
Chair: George Milne, U South Australia

J.Gause, P.Cheung, W.Luk, IC London <i>Static and Dynamic Reconfigurable Designs for a 2D Shape-Adaptive DCT</i>	14.00 - 14.25
R.Sidhu, S.Wadhwa, A.Mei, V.Prasanna, USC <i>A Self-Reconfigurable Gate Array Architecture</i>	14.25 - 14.50
H.Simmler, L.Levinson, R.Männer, U Mannheim <i>Multitasking on FPGA Coprocessors</i>	14.50 - 15.15
M.Vasilko, Bournemouth U <i>Design Visualisation for Dynamically Reconfigurable Systems</i>	15.15 - 15.40
D.Robinson, P.Lysaght, U Strathclyde <i>Verification of Dynamically Reconfigurable Logic</i>	15.40 - 16.05

16:05 - 16:30 COFFEE BREAK

16:30 - 18:35 TECHNOLOGY MAPPING AND R&P
Chair: John McCanny, The Queen's U

S.Krishnamoorthy, S.Swaminathan, R.Tessier, U Massachusetts <i>Area-Optimized Technology Mapping for Hybrid FPGAs</i>	16.30 - 16.55
J.Abke, E.Barke, U Hannover <i>CoMGen: Direct Mapping of Arbitrary Components into LUT-Based FPGAs</i>	16.55 - 17.20
S.Chandra Jain, A.Kumar, S.Kumar, IIT New Delhi <i>Efficient Embedding of Partitioned Circuits onto Multi-FPGA Boards</i>	17.20 - 17.45
J. Anderson, J.Saunders, S.Nag, C.Madabhushi, R.Jayaraman, Xilinx, Inc. <i>A Placement Algorithm for FPGA Designs with Multiple I/O Standards</i>	17.45 - 18.10
H.Kropp, C.Reuter, U Hannover <i>A Mapping Methodology for Code Trees onto LUT-based FPGAs</i>	18.10 - 18.35

18:35 - 19:30 BREAK

19:30 BANQUET, for details see page 19

Converging Media create new opportunities and new necessities for reconfigurable IPs. Reconfigurability is needed for mass production of flexible multi-standard wireless low power products, adaptable to support evolving standards.

Reconfigurability is needed to meet the demand by zillions of subscribers preferring individual media mixes from a growing number of different kinds of services. Don't miss the Tuesday keynote!

10:30 - 11:00 COFFEE BREAK

11:00 - 12:40 DYNAMICALLY RECONFIGURABLE 2
Chair: Patrick Lysaght, Strathclyde U

S.McMillan, S.Guccione, Xilinx Inc. <i>Partial Run-Time Reconfiguration Using JRTR</i>	11.00 - 11.25
X.Zhang, K.Ng, U Hong Kong <i>A Combined Approach to High-level Synthesis for Dynamically Reconfigurable Systems</i>	11.25 - 11.50
T.Rissa, J.Niittylahti, Tampere U <i>A Hybrid Prototyping Platform for Dynamically Reconfigurable Designs</i>	11.50 - 12.15
H.ElGindy, M.Middendorf, H.Schmeck, B.Schmidt, U Karlsruhe <i>Task Rearrangement on Partially Reconfigurable FPGAs with Restricted Buffer</i>	12.15 - 12.40

12:40 - 14:00 LUNCH BREAK

Molecular Biology goes Reconfigurable.

Fluidic FPGAs? The technology is available (patents pending). The ultimate accelerator for DNA sequencing? Don't miss the Tuesday plenum session !

**MONDAY, AUGUST 28
POSTERS**

14:00 - 16:05 POSTER PRESENTATIONS 1

Chair: Jürgen Becker, U Darmstadt

Christian Siemers, U of Applied Science, Heide
Reconfigurable Computing between Classification and Metrics - The Approach of Space/Time-Scheduling

Winnie W. Cheng, Steven J.E. Wilton, Babak Hamidzadeh, U British Columbia
FPGA Implementation of a Prototype WDM On-Line Scheduler

J.Hildebrandt, D.Timmermann, U Rostock
An FPGA Based Scheduling coprocessor for Dynamic Priority Scheduling in Hard Real-Time Systems

S.Sawitzki, J.Schönherr, R.Spallek, B.Straube, IIS Erlangen
Formal Verification of a Reconfigurable Microprocessor

R.Gadea, V.Herrero, A.Sebastia, A.Mocholí, U Valencia
The Role of the Embedded Memories in the Implementation of Artificial Neural Networks

G.Lafayette, ATMEL ES2 GmbH
Programmable System Level Integration brings System-on-Chip Design to the Desktop

A.Hilton, J.Hall, The Open University
On Applying Software Development Best Practice to FPGAs in Safety-Critical Systems

B.Blodget, Xilinx Inc.
Pre-Route Assistant: A Routing Tool for Run-Time Reconfiguration

T.Kobori, T.Maruyama, T.Hoshino, U Tsukuba
High Speed Computation of Lattice Gas Automata with FPGA

T.Shiozawa, N.Imlig, K.Nagami, K.Oguri, A.Nagoya, H.Nakada, NTT
An Implementation of Longest Prefix Matching for IP Router on Plastic Cell Architecture

B.Matasaru, T.Jebelean, RISC-Linz
FPGA Implementation of an Extended Binary GCD Algorithm for Systolic Reduction of Rational Numbers

16.05 - 16.30 COFFEE BREAK

**MONDAY - SOCIAL PROGRAM /
BANQUET**

19:30 BANQUET AT THE PARKHOTEL

The *Parkhotel*, where the conference banquet will be held, was the leading hotel in Carinthia dating back to the Austrian-Hungarian monarchy and centre of the social life in Carinthia. Three years ago the building was renovated and the former lobby and ballroom serve today as conference and banquet facility.

E-MAIL / WWW FACILITIES

About 10 PCs will be available for e-mail processing and browsing.

TRAVELLING TO VILLACH

NON-STOP FLIGHTS TO KLAGENFURT AIRPORT

SUMMER 2000 - ARRIVALS 27-05-00 - 28-10-00					
Changes without notice! - Warranty Disclaimer! Check: http://www.klagenfurt-airport.at/english/linienfluege.htm					
Origin	Flight	Departure	Arrival	Days	
Frankfurt	FRA V0484	11.30	13.05	1 2 3 4 5 6 7	
	V0486	16.25	18.00	1 2 3 4 5 6 7	
	V0488	21.10	22.45	1 2 3 4 5 6 7	
München (Munich)	MUC KL3201	09.40	10.40	1 2 3 4 5 - 7	
	KL3203	18.50	19.50	1 2 3 4 5 - 7	
Wien (Vienna)	VIE V0550/OS950	07.25	08.15	1 2 3 4 5 - -	
	V0552/OS952	10.40	11.30	1 2 3 4 5 6 7	
	V0554/OS954	13.50	14.50	1 2 3 4 5 - -	
	V0556/OS955	17.10	18.00	1 2 3 4 5 6 7	
	V0558/OS958	19.50	20.45	1 2 3 4 5 6 7	
	V0560/OS960	22.35	23.25	1 2 3 4 5 - 7	
Zürich	ZRH LX426	16.45	17.55	1 2 3 4 5 - 7	
	LX424	11.15	12.40	- - - - - 6 -	

More Flights: Amsterdam, Hamburg, Köln (Cologne), Linz, Salzburg

for Departures see page 25. A conference shuttle service to Villach will be provided on Saturday and Sunday

FPL 2000 — Registration Form

Please type or print clearly

Name: _____
(Family name) (First and Middle)

Affiliation: _____

Address: _____

Country: _____

Phone: _____

Fax: _____

E-mail: _____

Hotel reservation:

***(on request) ___ single room EUR 40 - 55
 ___ double room EUR 60 - 80

**** ___ single room EUR 55 - 80
 ___ double room EUR 80 - 120

***** (on request) ___ single room EUR 80 - 100
 ___ double room EUR 120 - 150

Date of arrival: ___/___/___ Date of departure: ___/___/___

Registration fees

- Early Registration Fee (until July, 30) 375 Euro
Includes attendance to all sessions, lunches, social program, banquet and workshop proceedings.
- Late Registration Fee (after July, 30) 410 Euro
Includes attendance to all sessions, lunches, social program, banquet and workshop proceedings.
- Fee for graduate students 200 Euro
Includes attendance to all sessions, lunches, and workshop proceedings
- Spouse / Partner fee 100 Euro
Includes social program and banquet.
- Exhibitor's fee 600 Euro
Includes everything as normal fee (for one person) plus exhibition space for the duration of the workshop.

Excursions on Sunday, Aug. 27:
 (incl. Bus, guide, entrance fees & lunch)

Scenic Tour Carinthia,
 Departure: 08:30 --- Return: 18:00
 Price/person: EUR 50 ___ Person(s) ___ Euro

Trip to Salzburg
 Departure: 08:00 --- Return: 21:00
 Price/person: EUR 100 ___ Person(s) ___ Euro

Trip to Venice
 Departure: 07:00 --- Return: 21:00
 Price/person: EUR 100 ___ Person(s) ___ Euro

Total amount: _____ Euro

Payment should be made in advance. Please select one:

Transfer directly to FPL 2000 bank account (Euro)
Bank account:
 FPL2000
 Creditanstalt Villach
 Sort Code: 11810
 Account Number: 01814432900
 SWIFT CABVATWW
please specify: "FPL 2000 & delegate name"

VISA Eurocard/Mastercard

Credit card number: _____
 Name of holder: _____
 Expiration date: _____
 Signature of holder: _____

Important: Any bank charges must be paid by the sender. The amount arriving at our bank must not be less than the registration fee. Please take care that any banking fees are settled.

With my signature I explicitly accept all booking and cancellation conditions, mentioned on this Registration Form (page 15: backside of this leaf).

Date and Signature: _____

**Please send or fax
 in advance to the
 General Chairman**
 FAX: +43 4242 2004 179