

Monday, Aug. 28		Tuesday, Aug. 29		Wednesday, Aug. 30	
<p>9:00 - 10:30 Plenum Session 1</p> <p>9:00 Welcome and Opening</p> <p>9:15 Keynote: Tsugio Makimoto, Hitachi, Tokyo <i>The Rising Wave of Field-Programmability</i></p> <p>10:00 Sriram Govindarajan, Ranga Vemuri, U Cincinnati <i>Tightly Integrated Design Space Exploration with Spatial and Temporal Partitioning in SPARCS</i></p>		<p>8:30 - 10:30 Plenum Session 2</p> <p>8:30 Keynote: Jan Rabaey, UC Berkeley <i>Silicon platforms for the next generation wireless systems - What role does reconfigurable hardware play?</i></p> <p>9:15 Invited Paper: John McCaskill, Patrick Wagler, GMD, Sankt Augustin <i>From reconfigurability to evolution in construction systems - spanning electronic, microfluidic and biomolecular domains.</i></p> <p>10:00 Invited Paper: M.Renovell, LIRMM, U Montpellier <i>An attempt to define a structural testing approach for RAM based FPGAs</i></p>		<p>8:30 - 10:30 Plenum Session 3</p> <p>8:30 Keynote: Tom Kean, Algotronix <i>It's FPL, Jim - but not as we know it! Market Opportunities for the new Commercial Architectures</i></p> <p>9:15 Invited Paper: Hideharu Amano, Yuichiro Shibata, Masaki Uno, Keio U, Yokohama <i>Reconfigurable Systems: New Activities in Asia</i></p> <p>10:00 Oskar Mencer, Heiko Huebert, Patrick Hung, Martin Morf, Michael J. Flynn, Stanford U <i>SiReAm: Object-Oriented Programming of Stream Architectures using PAM-Blox</i></p>	
10:30 - 11:00 Coffee Break		10:30 - 11:00 Coffee Break		10:30 - 11:00 Coffee Break	
<p>11:00 - 12:40 Network Processors</p> <p>J.Ditmar, K.Torkelson, A.Jantsch, Ericsson: <i>A Dynamically Reconfigurable FPGA-based Content Addressable Memory for Internet Protocol Characterization</i></p> <p>X.Tang, M.Aalsma, Chameleon Systems, Inc. <i>A Compiler Directed Approach to Hiding Configuration Loading Latency in Chameleon Reconfigurable Chips</i></p> <p>M.Iliopoulos, T.Antonakopoulos, U Patras <i>Reconfigurable Network Processors based on Field Programmable System Level Integrated Circuits</i></p> <p>H.Faloutsos, M.Smith, Xilinx, Inc. <i>Internet Connected FPL</i></p>	<p>11:00 - 12:40 Prototyping</p> <p>F.Renner, J.Becker, M.Glesner, U Darmstadt <i>Field Programmable Communication Emulation and Optimization for Embedded System Design</i></p> <p>H.Krupnova, G.Saucier, INP Grenoble/CSI <i>FPGA-Based Emulation: Industrial and Custom Prototyping Solutions</i></p> <p>R.Kress, A.Pytl, A.Sedlmeier, Infineon Technologies AG <i>FPGA-based Prototyping for Product Definition</i></p> <p>E.Canto, J.Moreno, J.Cabestany, I.Lacadena, J.Insenser, TU of Catalunya, Barcelona <i>Implementation of Virtual Circuits by Means of the FIPSOC Devices</i></p>	<p>11:00 - 12:40 Mobile Communication</p> <p>J.Becker, T.Pionteck, M.Glesner, U Darmstadt <i>DReAM: A Dynamically Reconfigurable Architecture for Future Mobile Communication Applications</i></p> <p>A.Blaickner, O.Nagy, H.Gruenbacher, CTI, Villach <i>Fast carrier and Phase Synchronization Units for Digital Receivers Based on Re-configurable Logic</i></p> <p>X.Reves, A.Gelonch, F.Casadevall, PU of Catalonia, Barcelona - <i>Software Radio Reconfigurable Hardware</i></p> <p>J.Ramirez, A.Garcia, P.Fernandez, L.Parrilla, A.Lloris, U Granada <i>Analysis of RNS-FPL Synergy for High Throughput DSP Applications: Discrete Wavelet Transform</i></p>	<p>11:00 - 12:40 Dynamically Reconfigurable II</p> <p>S.McMillan, S.Guccione, Xilinx Inc. <i>Partial Run-Time Reconfiguration Using JTRT</i></p> <p>X.Zhang, K.Ng, U Hong Kong <i>A Combined Approach to High-level Synthesis for Dynamically Reconfigurable Systems</i></p> <p>T.Rissa, J.Niitylahti, Tampere U <i>A Hybrid Prototyping Platform for Dynamically Reconfigurable Designs</i></p> <p>H.Elgindy, M.Middendorf, H.Schmuck, B.Schmidt, U Karlsruhe <i>Task Rearrangement on Partially Reconfigurable FPGAs with Restricted Buffer</i></p>	<p>11:00 - 12:40 Architectures</p> <p>E.Caspi, M.Chu, R.Huang, J.Yeh, A.DeHon, J.Wawrzynek, UC Berkeley <i>Stream Computations Organized for Reconfigurable Execution(SCORE): Introduction and Tutorial</i></p> <p>H.Lange, A.Koch, TU Braunschweig <i>Memory Access Schemes for Reconfigurable Processors</i></p> <p>A.Doering, G.Lustig, Medizinische U Luebeck <i>Generating Addresses for Multi-dimensional Array Access in FPGA On-chip Memory</i></p> <p>A.Derbyshire, W.Luk, IC London <i>Combining serialisation and Reconfiguration for FPGA Designs</i></p>	<p>11:00 - 12:40 Methodology and Technology</p> <p>G.Constantinides, P.Cheung, W.Luk, IC London <i>Multiple Resource Binding</i></p> <p>M.Vasilko, G.Benyon-Tinker, Bournemouth U <i>Automatic Temporal Floorplanning with Guaranteed Solution Feasibility</i></p> <p>K.Aoyama, H.Sawada, A.Nagoya, K.Nakajima, NTT Labs. <i>A Threshold Logic-based Reconfigurable Element with a Novel Programming Technology</i></p> <p>A.Krasniewski, Warsaw U <i>Exploiting Reconfigurability for Effective Detection of Delay Faults in LUT-Based FPGAs</i></p>
12:40 - 14:00 Lunch Break		12:40 - 14:00 Lunch Break		12:40 - 14:00 Lunch Break	
<p>14:00 - 16:05 Dynamically Reconfigurable I</p> <p>J.Gause, P.Cheung, W.Luk, IC London <i>Static and Dynamic Reconfigurable Designs for a 2D Shape-Adaptive DCT</i></p> <p>R.Sidhu, S.Wadhwa, A.Mei, V.Prasanna, USC <i>A Self-Reconfigurable Gate Array Architecture</i></p> <p>H.Simmler, L.Levinson, R.Maenner, U Mannheim <i>Multifunctional programmable single-board CAN monitoring module</i></p> <p>M.Vasilko, Bournemouth U <i>Design Visualisation for Dynamically Reconfigurable Systems</i></p> <p>D.Robinson, P.Lysaght, U Strathclyde <i>Verification of Dynamically Reconfigurable Logic</i></p>	<p>14:00 - 16:05 Student Papers</p> <p>T.Bartzick, M.Henze, J.Kickler, K.Woska, U Siegen <i>Design of a Fault-Tolerant FPGA</i></p> <p>R.McCready, U Toronto <i>Real-Time Face Detection on a Configurable Hardware System</i></p> <p>P.Pfeifer, TU Prague <i>Multifunctional programmable single-board CAN monitoring module</i></p> <p>P.Tomaszewicz, Warsaw U <i>Self-Testing of Linear Segments in User-Programmed FPGAs</i></p> <p>G.Lias Villar, U Vigo <i>Implementing a Fieldbus Interface Using a FPGA</i></p>	<p>14:00 - 16:05 Design Space Exploration</p> <p>R.Hartenstein, M.Herz, T.Hoffmann, U Nageldinger, U Kaiserslautern <i>Generation of Design Suggestions for Coarse-Grain Reconfigurable Architectures</i></p> <p>P.Heysters, J.Smit, G.Smit, P.Havinga, U Twente <i>Mapping of DSP Algorithms on Field Programmable Function Arrays</i></p> <p>D.Stefanovic, M.Martonosi, Princeton U <i>On Availability of Bit-narrow Operations in General-purpose Applications</i></p> <p>R.Grover, W.Shang, Q.Li, Santa Clara U <i>A Comparison of Bit-level and Word-level Matrix Multipliers</i></p> <p>F.Wolz, R.Kolla, U Wuerzburg <i>A new Floorplanning Method for FPGA Architectural Research</i></p>	<p>14:00 - 16:05 Student Papers</p> <p>S.Wadhwa, A.Dandalis, USC <i>Efficient Self-Reconfigurable Implementations Using On-Chip Memory</i></p> <p>A.Glasmacher, K.Woska, U Siegen <i>Design and Implementation of a XC6216 FPGA Model in Verilog</i></p> <p>J.Andreas, U Ljubljana <i>Reusable DSP Functions in FPGAs</i></p> <p>M.Redekopp, USC LA <i>A Parallel Pipelined SAT Solver for FPGAs</i></p> <p>A.Touhafi, U Brussels <i>A Multi-Node Dynamic Reconfigurable Computing System with distributed reconfiguration control</i></p>	<p>14:00 - 15:40 Compilation and Related Issues</p> <p>A.Takayama, Y.Shibata, K.Iwai, H.Amano, Keio U <i>Datallow Partitioning and Scheduling Algorithms for WASMII, a Virtual Hardware</i></p> <p>B.Kastrup, J.Trum, O.Moreira, J.Hoogerbrugge, J.V.Meerbergen, Philips Laboratories <i>Compiling Applications for ConCISE: An Example of Automatic HW/SW Partitioning and Synthesis</i></p> <p>O.Diesel, G.Milne, U South Australia, Adelaide <i>Behavioral Language Compilation with Virtual Hardware Management</i></p> <p>V.Sklyarov, U Aveiro - <i>Synthesis and Implementation of RAM-based Finite State Machines in FPGAs</i></p>	<p>14:00 - 15:40 Applications II</p> <p>S.Ichikawa, H.Saito, L.Udorn, K.Konishi, Toyohashi U <i>Evaluation of Accelerator Designs for Subgraph Isomorphism Problem</i></p> <p>M.Edwards, P.Green, UMIST <i>The Implementation of Synchronous Datallow Graphs Using Reconfigurable Hardware</i></p> <p>T.Courtney, R.Turner, R.Woods, Queens U Belfast <i>A New Coding System for Use with Reconfigurable Filters</i></p> <p>C.Bobda, T.Lehmann, Paderborn U <i>Efficient Building of Word Recognizer in FPGAs for Term-Document Matrices Construction</i></p>
16:05 - 16:30 Coffee Break		16:05 - 16:30 Coffee Break		16:05 - 16:30 Coffee Break	
<p>16:30 - 18:35 Technology Mapping and R&P</p> <p>S.Krishnamoorthy, S.Swaminathan, R.Tessier, U Massachusetts <i>Area-Optimized Technology Mapping for Hybrid FPGAs</i></p> <p>J.Abke, E.Barke, U Hannover <i>ComGen: Direct Mapping of Arbitrary Components into LUT-Based FPGAs</i></p> <p>S.Chandra Jain, A.Kumar, S.Kumar, IIT New Delhi <i>Efficient Embedding of Partitioned Circuits onto Multi-FPGA Boards</i></p> <p>J.Anderson, J.Saunders, S.Nag, C.Madabhushi, R.Jayaraman, Xilinx, Inc. <i>A Placement Algorithm for FPGA Designs with Multiple I/O Standards</i></p> <p>H.Kropp, C.Reuter, U Hannover - <i>A Mapping Methodology for Code Trees onto LUT-based FPGAs</i></p>	<p>16:30 - 18:35 Biologically Inspired Methods</p> <p>J.Torresen, U Oslo <i>Possibilities and Limitations of Applying Evolvable Hardware to Real-World Applications</i></p> <p>Y.Yamaguchi, A.Miyashita, T.Maruyama, T.Hoshino, U Tsukuba <i>A Co-processor System with a Virtex FPGA for Evolutionary Computation</i></p> <p>C.Bauer, P.Zipf, H.Wojtkowiak, U Siegen <i>System Design with Genetic Algorithms</i></p> <p>J.Zhu, G.Milne, U of South Australia, Adelaide <i>Implementing Kak Neural Networks on a Reconfigurable Platform</i></p> <p>S.Maya, R.Reynoso, C.Torres, M.Arias-Estrada, INAOC Puebla - <i>Compact Spiking Neural Network Implementation in FPGA</i></p>	<p>16:30 - 18:35 Applications I</p> <p>O.Yamamoto, Y.Shibata, H.Kurosawa, H.Amano, Tokyo Denki U - <i>A Reconfigurable Stochastic Model Simulator for analysis of parallel systems</i></p> <p>S.Bellis, W.Marnane, NMRC, Cork <i>A CORDIC Arc tangent FPGA Implementation for a High-Speed 3D-Camera System</i></p> <p>S.Melnikoff, P.James-Roxby, S.Quigley, M.Russell, U Birmingham - <i>Reconfigurable Computing for Speech Recognition: Preliminary Findings</i></p> <p>H.Ploog, M.Schmalisch, D.Timmermann, U Rostock <i>Security Upgrade of Existing ISDN Devices by Using Reconfigurable Logic</i></p> <p>T.Miomo, K.Yasuoka, M.Kanazawa, Kyoto U <i>The Fastest Multiplier on FPGAs with Redundant Binary Representation</i></p>	<p>16:30 - 18:35 Optimization</p> <p>R.Enzler, T.Jeger, D.Cottel, G.Troester, ETH Zurich <i>High Level Area and Performance Estimation of Hardware Building Blocks on FPGAs</i></p> <p>R.Tessier, H.Giza, U Massachusetts <i>Balancing Logic Utilization and Area Efficiency in FPGAs</i></p> <p>J.Emmert, J.Cheatham, P.Kataria, C.Stroud, M.Abramovici, U Kentucky <i>Predicting Performance Penalty for fault Tolerance in Routing Self-Testing Areas (STARs)</i></p> <p>J.Qiao, M.Keda, K.Asada, U Tokyo <i>Optimum Functional Decomposition for LUT-based FPGA Synthesis</i></p> <p>M.Eisenring, M.Platzner, ETH Zurich <i>Optimization of Run-time Reconfigurable Embedded Systems</i></p>	<p>14:00 - 15:40 Compilation and Related Issues</p> <p>A.Takayama, Y.Shibata, K.Iwai, H.Amano, Keio U <i>Datallow Partitioning and Scheduling Algorithms for WASMII, a Virtual Hardware</i></p> <p>B.Kastrup, J.Trum, O.Moreira, J.Hoogerbrugge, J.V.Meerbergen, Philips Laboratories <i>Compiling Applications for ConCISE: An Example of Automatic HW/SW Partitioning and Synthesis</i></p> <p>O.Diesel, G.Milne, U South Australia, Adelaide <i>Behavioral Language Compilation with Virtual Hardware Management</i></p> <p>V.Sklyarov, U Aveiro - <i>Synthesis and Implementation of RAM-based Finite State Machines in FPGAs</i></p>	<p>14:00 - 15:40 Applications II</p> <p>S.Ichikawa, H.Saito, L.Udorn, K.Konishi, Toyohashi U <i>Evaluation of Accelerator Designs for Subgraph Isomorphism Problem</i></p> <p>M.Edwards, P.Green, UMIST <i>The Implementation of Synchronous Datallow Graphs Using Reconfigurable Hardware</i></p> <p>T.Courtney, R.Turner, R.Woods, Queens U Belfast <i>A New Coding System for Use with Reconfigurable Filters</i></p> <p>C.Bobda, T.Lehmann, Paderborn U <i>Efficient Building of Word Recognizer in FPGAs for Term-Document Matrices Construction</i></p>
18:35 - 19:30 Break		18:35 - 19:30 Break		18:35 - 19:30 Break	
19:30 Banquet at the Parkhotel		19:30 Boat trip on lake Ossiach with dinner		19:30 Closing Session	
<p>Sunday, Aug. 27</p> <p>19:30 - 21:00 Welcome cocktail and registration at the Congress Center Villach</p>		<p>Optional Excursions on Sunday: (min. 15 Persons per excursion required, see Registration Form on the back side)</p> <ul style="list-style-type: none"> - Scenic Tour Carinthia - Trip to Salzburg - Trip to Venice 		<p>Poster Sessions</p> <p>Monday, 14:00 - 16:05</p> <p>Christian Siemens, U of Appl.Sc. Heide <i>Reconfigurable Computing between Classification and Metrics - The Approach of Space/Time-Scheduling</i></p> <p>Winnie W. Cheng Steven J.E. Wilton, Babak Hamidzadeh, U British Columbia <i>FPGA Implementation of a Prototype WDM On-Line Scheduler</i></p> <p>Hildebrandt, D.Timmermann, U Rostock <i>An FPGA Based Scheduling coprocessor for Dynamic Priority Scheduling in Hard Real-Time Systems</i></p> <p>S.Sawitzki, J.Schoenherr, R.Spallek, B.Straube, IIS Erlangen <i>Formal Verification of a Reconfigurable Microprocessor</i></p> <p>R.Girones, V.Bosch, A.Cortes, A.Salcedo, U Valencia <i>The Role of the Embedded Memories in the Implementation of Artificial Neural Networks</i></p> <p>J.Rosenberg, ATMEL ES2 GmbH - <i>Programmable System Level Integration brings System-on-Chip Design to the Desktop</i></p> <p>A.Hilton, J.Hall, The Open University - <i>On Applying Software Development Best Practice to FPGAs in Safety-Critical Systems</i></p> <p>B.Blodgett, Xilinx Inc. <i>Pre-Route Assistant: A Routing Tool for Run-Time Reconfiguration</i></p> <p>T.Kobori, T.Maruyama, T.Hoshino, U.Tsukuba <i>High Speed Computation of Lattice Gas Automata with FPGA Driven Multi-Context Schedulers</i></p> <p>T.Shiozawa, N.Imig, K.Nagami, K.Oguri, A.Nagoya, H.Nakada, NTT <i>An Implementation of Longest Prefix Matching IP Router on Plastic Cell Architecture</i></p> <p>B.Malasar, T.Jebelean, RISC-Linz <i>FPGA Implementation of an Extended Binary GCD Algorithm for Systolic Reduction of Rational Numbers</i></p> <p>Tuesday, 14:00 - 16:05</p> <p>L.Sekanina, A.Silame, Brno U <i>Toward Uniform Approach to Design of Evolvable Hardware Based System</i></p> <p>A.Trost, A.Zemva, B.Zajc, U Ljubljana <i>Educational Programmable Hardware Prototyping and Verification System</i></p> <p>R.Hoffmann, B.Ulmann, K.-P.Voelkmann, S.Waldschmidt, Darmstadt U - <i>A Stream Processor Architecture Based on the Configurable CEPRA-S</i></p> <p>U.Hatnik, P.Schwarz, FHG Dresden <i>An Innovative Approach to Couple EDA Tools with Reconfigurable Hardware</i></p> <p>K.Tammemae, T.Evartson, TTU - <i>FPL Curriculum at TTU</i></p> <p>J.-M.Raczinski, S.Sladek, CEMAMU, France Telecom R&D <i>The modular architecture of SYNTHUP, FPGA based PCB board for real-time sound synthesis and digital signal processing</i></p> <p>A.Brinkmann, D.Langen, U.Rueckert, Paderborn U <i>A Rapid Prototyping Environment for Microprocessor based System-on-Chip and its Application to the Development of a Network Processor</i></p> <p>J.Noguera, R.Badia, U Autonomia de Barcelona <i>Configuration Prefetching for Non-Deterministic Event Driven Multi-Context Schedulers</i></p> <p>C.Phillips, Chameleon Systems, Inc. <i>cdma2000 Wireless Application on the CS2112 Reconfigurable Hardware Platform</i></p> <p>E.Fabiani, D.Lavenier, IRISA <i>Placement of Linear Array</i></p>	

Conference Date: 27. - 30. August 2000

CANCELLATION AND REFUND POLICY - HOTEL RESERVATIONS
Booking of accommodation is binding.

Cancellation before 15 August 2000: no charges

Cancellation after 15 August 2000: The amount for one night will be deducted from your credit card.

Furthermore, the hotel is legally entitled to charge the customer for the stay booked at the hotel in case of cancellation after August 25, respectively in case of no-show. Cancellations have to be made in writing to the Congress Secretariat.

CHANGES / MODIFICATIONS - HOTEL RESERVATION

Modifications have to be made in writing. Within the second changes of reservation a handling fee of EUR 15.00 will be charged by the Villach Tourism GmbH.

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Before 1 August 2000 Full refund less EUR 35,00 handling fee

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After 15 August 2000 No refund

Refunds will be issued after the congress. Requests for a refund must be made in writing to the FPL'2000 Conference Secretariat.

Please send or fax, in advance, the Registration Form/ Enquiries to the General Chairman.

General Chair:

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FPL 2000 — Registration Form

Please type or print clearly

Name: _____
(Family name) (First and Middle)

Affiliation: _____

Address: _____

Country: _____

Phone: _____

Fax: _____

E-mail: _____

Hotel reservation:

***(on request): _____ single room EUR 40 - 55

_____ double room EUR 60 - 80

****: _____ single room EUR 55 - 80

_____ double room EUR 80 - 120

***** (on request): _____ single room EUR 80 - 100

_____ double room EUR 120 - 150

Date of arrival: __/__/__ Date of departure: __/__/__

Registration fees

Early Registration Fee (until July, 30) 375 Euro
Includes attendance to all sessions, lunches, social program, banquet and workshop proceedings.

Late Registration Fee (after July, 30) 410 Euro
Includes attendance to all sessions, lunches, social program, banquet and workshop proceedings.

Fee for graduate students 200 Euro
Includes attendance to all sessions, lunches, and workshop proceedings

Spouse / Partner fee 100 Euro
Includes social program and banquet.

Exhibitor's fee 600 Euro
Includes everything as normal fee (for one person) plus exhibition space for the duration of the workshop.

**Excursions on Sunday, Aug. 27:
(incl. Bus, guide, entrance fees & lunch)**

Scenic Tour Carinthia, 08:30 - 18:00
Price/person: EUR 50 _____ Person(s) _____ Euro

Trip to Salzburg, 08:00 - 21:00
Price/person: EUR 100 _____ Person(s) _____ Euro

Trip to Venice, 07:00 - 21:00
Price/person: EUR 100 _____ Person(s) _____ Euro

Total amount: _____ Euro

Payment should be made in advance. Please select one:

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Bank account:

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Important: Any bank charges must be paid by the sender. The amount arriving at our bank must not be less than the registration fee. Please take care that any banking fees are settled.

With my signature I explicitly accept all booking and cancellation conditions, mentioned on this Registration Form.

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**Please send or fax in advance
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FAX: +43 4242 2004 179