



FPL '98

Eighth International Workshop on Field Programmable Logic and Applications Advance Program

http://xputers.informatik.uni-kl.de/FPL/index_fpl.html



UNIVERSITY OF
KAISERSLAUTERN

Tallinn Technical University, Raja 15, EE0026 Tallinn, Estonia
Conference Venue: Tallinn National Library, Tõnismägi 2, EE0100 Tallinn, Estonia

Sunday, Aug. 30

20.00 Informal Gathering and Registration at the
Hotel Viru (lobby)

Monday, Aug. 31

8.00 - 9.00 Registration at Tallinn National Library

9.00 - 9.20 Opening Session

9.20 - 10.20 Keynote

V. Milutinovic, University of Belgrade:
Key Issues in Reconfigurable Computing

10.20 - 10.35 Coffee Break

10.35 - 12.15 Session 1: *Design Methods*

D. Robinson, P. Lysaght, G. McGregor, U. Strathclyde:
New CAD Framework Extends Simulation of Dynamically Reconfigurable Logic

W. Luk, S. McKeever, IC London:

Pebble: A Language For Parametrised and Reconfigurable Hardware Design

V. Sklyarov, R. Sal Monteiro, N. Lau, A. Melo, A. Oliveira, K. Kondratjuk, Aveiro U:

Integrated Development Environment for Logic Synthesis of Digital Circuits Based on Dynamically Reconfigurable FPGAs

R. Hartenstein, M. Herz, F. Gilbert, U. Kaiserslautern:
Designing for the Xilinx XC6200 FPGAs

12.15 - 13.30 Lunch

13.30 - 15.10 Session 2: *General Aspects*

J. Becker, A. Kirschbaum, F.-M. Renner, M. Glesner, TU Darmstadt:
Perspectives of Reconfigurable Computing in Research, Industry and Education

G. Brebner, U. Edinburgh:

Field-Programmable Logic: Catalyst for New Computing Paradigms

W. Luk, N. Shirazi, P. Y. K. Cheung, IC London:

Run-time management of partially-reconfigurable designs

M. Platzner, G. De Micheli, Stanford U:
Acceleration of Satisfiability Algorithms by Reconfigurable Hardware

15.10 - 15.30 Coffee Break

15.30 - 17.10 Session 3: *Prototyping / Simulation*

J. Stohmann, K. Harbich, M. Olbrich, E. Barke, U. Hannover:

An Optimized Design Flow for Fast FPGA-Based Rapid Prototyping

H. Krupnova, G. Saucier, INP Grenoble:

A Knowledge-Based System for Prototyping on FPGAs

R. Macketanz, W. Karl, TU Munich:

JVX - A Rapid Prototyping System Based on Java and FPGAs

J. Shetler, B. Hemme, C. Yang, C. Hinsz, Cal Poly:

Prototyping New ILP Architectures Using FPGAs

18.30 Reception at Tallinn Town Hall

Tuesday, Sep. 1

8.30 - 10.10 Session 4: *Development Methods*

Samary Baranov, Ben Gurion U Negev:

CAD System for ASM and FSM Synthesis

J. M. Emmert, A. Randhar, D. Bhatia, U. Cincinnati:

Fast Floorplanning for FPGAs

M. Renovell, J. M. Portal, J. Figueras, Y. Zorian, LIRMM-UM2:

SRAM-Based FPGAs: A Fault Model for the Configurable Logic Modules

G. Haug, W. Rosenstiel, FZI Karlsruhe:

Reconfigurable Hardware as Shared Resource in Multipurpose Computers

10.10 - 10.35 Coffee Break

10.35 - 11.50 Session 5: *Accelerators*

S. Robinson, M. Caffrey, M. Dunham, LANL

Reconfigurable Computer Array: The Bridge Between High Speed Sensors and Low Speed Computing

W. Luk, P. Andreou, N. Shirazi, D. Siganos, IC London:

A Reconfigurable Engine for Real-Time Video Processing

F.-M. Renner, J. Becker, M. Glesner, TU Darmstadt:

An FPGA Implementation of a Magnetic Bearing Controller for Mechatronic Applications

11.50 - 13.05 Session 6: *System Architectures*

R. Hartenstein, M. Herz, T. Hoffmann, U. Nageldinger, U. Kaiserslautern:

Exploiting contemporary memory techniques in reconfigurable accelerators

A. Donlin, U. Edinburgh:

Self Modifying Circuitry - A Platform for Tractable Virtual Circuitry

K. GajjalaPurna, K. Simha, D. Bhatia, U. Cincinnati:

REACT: Reactive Environment for Runtime Reconfiguration

13.05 - 14.20 Lunch

14.20 - 16.00 Session 7: *Applications*

S. Charlwood, P. James-Roxby, U. Birmingham:

Evaluation of the XC6200-series architecture for cryptographic applications

A. Zakerolhosseini, P. Lee, E. Horne, U. Kent:

An FPGA based object recognition machine

G. Acher, W. Karl, M. Leberrecht, TU Munich:

PCI-SCI Protocol Translations: Applying Microprogramming Concepts to FPGAs

T. Callahan, J. Wawrzyniec, UC Berkeley

Instruction-Level Parallelism for Reconfigurable Computing

14.20 - 15.35 Poster Introduction (parallel to S.7)

15.35 - 16.20 Session 8: *Poster Exhibition: see below*

16.20 - 16.40 Coffee Break

16.40 - 18.00 Session 9: *Hardware/Software Codesign*

G. McGregor, D. Robinson, P. Lysaght, U. Strathclyde:

A Hardware/Software Co-design Environment for Reconfigurable Logic Systems

K. Bondalapati, V. Prasanna, U. of Southern California:

Mapping Loops onto Reconfigurable Architectures

S. Asaad, K. Warren, IBM T.J. Watson Research Center:

Speed Optimization of the ALR circuit using an FPGA with embedded RAM: A Design Experience

19.30 Banquet at von Glehn's castle

Wednesday, Sep. 2

8.30 - 9.45 Session 10: *System Development*

R. Kress, A. Pyttel, A. Sedlmeier, Siemens AG:

High-level Synthesis for Dynamically Reconfigurable HW/SW-Systems

N. McKay, S. Singh, XILINX:

Dynamic Specialisation of XC6200 FPGAs by Partial Evaluation

S. Guccione, XILINX:

Webscope: A Circuit Debug Tool

9.45 - 10.00 Coffee Break

10.00 - 11.40 Session 11: *Algorithms on FPGAs*

D. Lavenier, Y. Saouter, IRISA-CNRS:

Computing Goldbach partitions using pseudo-random bit generator operators on a FPGA systolic array

P. Zhong, M. Martonosi, S. Malik, P. Ashar, Princeton U:

Solving Boolean Satisfiability with Dynamic Hardware Configurations

J. Pöldre, M. Mandre, K. Tammemäe, Tallinn Technical U:

Modular exponentiation realization on FPGA

B. Feher, G. Szedo, TU Budapest:

Cost effective 2x2 inner product processors

10.00 - 11.15 Poster Introduction (parallel to S.11)
11.15 - 12.00 Session 12:
Poster Exhibition: see below

12.00 - 13.00 Closing Session

T. Maruyama, T. Funatsu, T. Hoshino, U. of Tsukuba:

A Field-Programmable Gate-Array System for Evolutionary Computation

T. Miyazaki, K. Shirakawa, M. Katayama, T. Murooka,

A. Takahara, NTT:

A Transmutable Telecom System

Conclusions, Award Ceremony and Announcements

14.00 Tour to Lahemaa National Park,
visiting manors, and dinner in
Altja tavern

Thursday, Sep. 3

8.30 - 12.00 Tutorial at Tallinn Tech. University

B. Radunovic, V. Milutinovic, Univ. Belgrade:

A Survey of Reconfigurable Computing Architectures, Part 1

13.00 - 16.00 Tutorial at Tallinn Tech. University

B. Radunovic, V. Milutinovic, Univ. Belgrade:

A Survey of Reconfigurable Computing Architectures, Part 2

Posters (session 8)

N.L. Miller, S.F. Quigley, U. Birmingham:

A Novel Field Programmable Gate Array Architecture for high speed arithmetic processing

D. MacVicar, S. Singh, XILINX:

Accelerating DTP with Reconfigurable Computing Engines

C. N. Ojeda-Guerra, R. Esper-Chain, M. Estupinan, A. Suarez, U. Las Palmas:

Hardware Mapping of a Parallel Algorithm for Matrix-Vector Multiplication

G. Brebner, U. Edinburgh:

An Interactive Datasheet for the Xilinx XC6200

N. Woolfries, P. Lysaght, S. Marshall, G. McGregor, D. Robinson, U. Strathclyde:

Fast Adaptive Image Processing in FPGAs using Stack Filters

S. Sawitzki, A. Gratz, R. Spallek, U. Dresden:

Increasing Microprocessor Performance with Tightly-Coupled Reconfigurable Logic Arrays

N. Bergmann, P. Sutton, Queensland U:

A High-Performance Computing Module for a Low Earth Orbit Satellite using Reconfigurable Logic

S. Yamagawa, M. Ono, T. Yamazaki, P. Kulkasem, M. Hirota,

K. Wada, U. Tsukuba:

Maestro-Link: A High Performance Interconnect for PC Cluster

T. Shiozawa, K. Oguri, K. Nagami, H. Ito, R. Konishi, N. Imlig, NTT:

A Hardware Implementation of Constraint Satisfaction Problem Based on New Reconfigurable LSI Architecture

P. Merino, J. Lopez, M. Jacome, U. Politecnica de Madrid:

A Hardware Operating System for Dynamic Reconfiguration of FPGAs

E. Cerro-Prada, P. B. James-Roxby, U. Birmingham:

High speed low level image processing on FPGAs using distributed arithmetic

T.-T. Do, H. Kropp, C. Reuter, P. Pirsch, U. Hannover:

A Flexible Implementation of High-Performance FIR Filters on Xilinx FPGAs

I. Vassanyi, U. Veszprem:

Implementing processor arrays on FPGAs

S. Holmstrom, K. Sere, Abo Akademi U:

Reconfigurable Hardware - A Study in Codesign

C. Ackad, TU Braunschweig:

Statechart-based HW/SW-Codesign of a Multi-FPGA-Board and a Microprocessor

Posters (session 12)

A. Touhafi, W. F. Brissinck, E. F. Dirck, U. Brussel:

Simulation of ATM switches using Dynamically Reconfigurable FPGA's

T. Rissa, T. Mäkeläinen, J. Siirtola, J. Niitylahti, Tampere U:

Fast Prototyping Using System Emulators

A. Dandalis, V. Prasanna, U. of Southern California:

Space-efficient Mapping of 2D-DCT onto Dynamically Configurable Coarse-Grained Architectures

I. Lemberski, M. Ratniece, Riga Aviation U:

XILINX4000 Architecture-Driven Synthesis for Speed

V. Tomachev, Inst. of Eng. Cybernetics Belarus:

The PAL-implementation of Boolean function characterized by minimum delay

A. Abo Shosha, P. Reinhard, F. Rongen, Research Centre

Jülich:

Reconfigurable PCI-Bus Interface (RPCI)

A. Trost, A. Zemva, B. Zajc, U. Ljubljana:

Programmable Prototyping System for Image Processing

J. Fischer, C. Müller, H. Kurz, TU Aachen:

A Co-Simulation Concept for an Efficient Analysis of Complex Logic Designs

A. Döring, W. Obelöer, G. Lustig, Med. U. Lübeck:

Programming and Implementation of Reconfigurable Routers

M. Moure, U. Vigo:

Virtual Instruments based on reconfigurable logic

C. Siemers, D. Möller, FH Westküste:

The >S<puter: Introducing a Novel Concept for Dispatching Instructions Using Reconfigurable Hardware

L. Lagadec, B. Pottier, U. de Bretagne Occidentale:

A 6200 model and editor based on object technology

M. Eisenring, J. Teich, ETH Zürich:

Interfacing Hardware and Software

J. Hwang, E. Dellinger, S. Mitra, S. Mohan, C. Patterson,

R. Wittig, XILINX:

Generating Layouts for Self-Implementing Modules



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Advance Program

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Conference Survey								
Monday, Aug.31		Tuesday, Sep.1		Wednesday, Sep.2		Thursday, Sep.3		
8:00-9:00	Registration	8:30-10:10	Session 4	8:30-9:45	Session 10	8:30 -12:00 Tutorial (at Tallinn Tech. University) Reconfigurable Computing Architectures		
9:00-9:20	Opening session	10:10-10:35	Coffee Break	9:45-10:00	Coffee Break			
9:20-10:20	Keynote	10:35-11:50	Session 5	10:00-11:15	Poster Intro	11	Reconfigurable Computing Architectures	
10:20-10:35	Coffee Break	11:50-13:05	Session 6	11:15-12:00	Session 12			
10:35-12:15	Session 1	13:05-14:20	Lunch	12:00-13:00 Closing Session		13:00 - 16:00 Tutorial (at Tallinn Tech. University) Reconfigurable Computing Architectures		
12:15-13:30	Lunch	14:20-15:35	Poster Intro	Tour to Lahemaa National Park, visiting manors and dinner in Altja tavern				
13:30-15:10	Session 2	15:35-16:20	Session 8					7
15:10-15:30	Coffee Break	16:20-16:40	Coffee Break					
15:30-17:10	Session 3	16:40-18:00	Session 9					
18:30	Reception at Town Hall	19:30	Banquet at von Glehn's castle					

General Chairman:

Prof. Andres Keevallik

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FPL'98 — Registration Form

Please type or print clearly

Name: _____
(Family name) (First and Middle)

Affiliation: _____

Address: _____

Country: _____

Phone: _____

Fax: _____

E-mail: _____

Registration fees

Normal fee 3200 EEK

Includes attendance to all sessions, lunches, social program, banquet and workshop proceedings.

Student fee 1600 EEK

Includes attendance to all sessions, lunches, and workshop proceedings

Spouse / Partner fee 800 EEK

Includes social program and banquet.

Exhibition fee 6400 EEK

Includes everything as normal fee (for one person) plus exhibition space for the duration of the workshop.

Total amount: _____ EEK

Please check, if you will join the tour on Wednesday

Payment should be made in advance, in EEK (8 EEK = 1 DM), DM, or USD . Please select one:

Bank transfer:

Common data to be specified for all three methods

Beneficiary's bank: EESTI UHISPANK, SWIFT: EEUH22X

Beneficiary's name: Andres Keevallik

please specify: "FPL'98 & delegate name"

Transfer directly to FPL'98 bank account (EEK):
Beneficiary's account: 10 0020 3734 2004

Transfer to correspondent bank account (USD):
Correspondent bank: Bankers Trust Co, NY, SWIFT: BKTRUS33
Beneficiary's account: 04-401-362

Transfer to correspondent bank account (DM):
Correspondent bank: Deutsche Bank, Fr., SWIFT: DEUTDEFF
Beneficiary's account: 10 0020 3734 2004

Cheque
Cheque in EEK made payable to Prof. Andres Keevallik,
please specify: "FPL'98 & delegate name"

VISA Eurocard/Mastercard

Credit card number: _____

Name of holder: _____

Expiration date: _____

Signature of holder: _____

Important: Any bank charges must be paid by the sender. The amount arriving at our bank must not be less than the registration fee. Please take care that any banking fees are settled.

Date and Signature: _____

Please send or fax by **August 1, 1998**
to the General Chairman. Fax: +372-6202246

FPL'98 — Hotel Reservation Form

Please type or print clearly

Name: _____
(Family name) (First and Middle)

Affiliation: _____

Address: _____

Country: _____

Phone: _____

Fax: _____

(Date)

(Stamp and signature)

Type of room:

- single room
- double room
- triple room

Preferred category:

- category I about 1600 EEK
- category II about 1100 EEK
- category III about 750 EEK
- student hotel about 150 EEK

Check in date: _____

Check out date: _____

Arrival time: _____

Arrival by: plane ferry car/bus/train

Deadline:
August 15, 1998

prices here are per
night in single room

Conference Hotline (from Aug. 15 to Sep. 4): +372-6202253