Abstract

Many of today's application areas require very high performance as well as a certain flexibility. It has shown, that the classic ways of realizing the associated algorithms, ASIC implementation and microprocessors, are often not adequate, as microprocessors cannot provide the performance, while ASIC implementations lack flexibility. As a third way of implementation, Reconfigurable Computing has gained importance in the recent years. Today countless applications are already implemented on reconfigurable architectures. While most implementations focus on the data manipulation part, storage and access of computation data is mostly an undervaluated topic. Since there is only a little work done in the area of data access, usually a straightforward application specific implementation is chosen to address computation data ignoring major topics like reconfiguration load, the memory interface performance, and overall design time.

Already for microprocessors the memory communication bandwidth has become worse and worse for each new technology generation. But for accelerators, especially for data-intensive applications, the memory communication bandwidth problem is drastically more dramatic than with microprocessor usage. Because reconfigurable computers a commonly based on a different computing paradigm as microprocessors, there are also new memory access optimization methods needed.

This thesis presents a data sequencing concept, which has been especially developed for reconfigurable computing. Besides the need of reconfigurable machines for small configuration sets, it addresses the memory communication performance problem with several strategies. An enhanced scheduling for data to be accessed is performed, where a trade-off between data processing time and memory interface speed is considered. The memory access speed may also be improved by modifying storage schemes. This takes several access optimizations based on a 2-dimensional memory organization into account. The result of this method is an overall decrease of memory cycles, independent from the utilized memory technology.

Under determination of several reconfigurable computer architectures the proposed data sequencing concept is the basis for different hardware implementations. Therefore a development framework has been implemented as an Internet-based software. It assists programming the data sequencer in all development phases with a comprehensive toolset. Besides several possibilities to enter applications, it provides different tools for program validation and application download. Further it supports public access to a prototype for testing purposes. Therefore the prototype has to be connected to a web server, which runs also the development system.