List of Symbols and Acronyms

Numerics

1d-GAG	:	1-dimensional generic address generator
2d	:	2-dimensional
2d-MB	:	2-dimensional multi bank
2d-MBB	:	2-dimensional multi bank burst mode

A

A	:	Address, or transformation matrix
AC	:	memory access cycles to reference all memory locations inside a scan window
ΔA	:	step width for Address modification
AE	:	address expression
AG	:	address generator
AGU	:	address generation unit
AIR	:	address instruction read access memory
ALU	:	arithmetic logic unit
API	:	application programming interface
APP	:	memory access cycles to reference all data of an application
AR	:	auxiliary register
ARAU	:	auxiliary register arithmetic unit
AS	:	address sequence
ASIC	:	application specific integrated circuit
ASU	:	application specific unit
AWT	:	abstract window toolkit

B

B	:	Base
B_0	:	initial Base value

ΔB : step width for Base modification

BCU : burst control unit

BEDO-DRAM : burst enhanced data out dynamic read access memory

BFU : basic function unit

BRAM : block read access memory

C

C : Ceiling (end value for Limit)

CAB : configurable analog block

cACU : custom address calculation unit

CAD : computer aided design

CAL : configurable array logic

CAM : content-addressable memory

CAU : configurable array unit

CC : control connection block

CCM : custom computing machine

CGI : common gateway interface

CHAMP : configurable hardware algorithm mappable preprocessor

CD : data connection block

CL : configurable logic

CLB : configurable logic block

CLK : clock

C.mmp : Computer.multi-mini-processor

cMMU : customized memory management unit

CoDe-X : Co-Design for Xputers

CoMPARE : common minimal processor architecture with reconfigurable extension

CP : computational processor

CPL : compiler mode bit

CPLD : complex programmable logic device

CPU : central processing unit

CSI : configurable system interconnect
CSL : configurable system logic
CSoC : configurable system-on-chip
CSSU : compare, select, store unit

D

D : distance
DAGEN : data-address generation logic
DARAM : dual-access read access memory
DCU : datapath control unit
DDR-SDRAM : double data rate synchronous dynamic read access memory
DISC : dynamic instruction set computer
DLL : delay-locked loop
DM : datapath module
DMA : direct memory access
DMC : digital macro cell
DMEM : data memory
DP : data-page pointer
DP-FPGA : datapath field programmable gate array
DPSS : datapath synthesis system
DPU : datapath unit
DRAM : dynamic read access memory
DReAM : dynamically reconfigurable architecture for mobile systems
DRC : design rule check
DSP : digital signal processor
DTI : data-transfer intensive

E

EA : effective address
EAB : embedded array block
EPLD : enhanced programmable logic device

ERC : electrical rule check

EU : execution unit

F

F : Floor (end value for Base)

FADC : flash analog digital converter

FCCM : FPGA-based custom computing machine

FDU : fetch and decode unit

FFT : fast fourier transformation

FIFO : first in first out

FLEX : flexible logic element matrix

FPGA : field programmable gate array

FPIC: : field programmable interconnect component

FPL : field programmable logic

FPU : floating point unit

FSM : finite state machine

FTP : file transfer protocol

G

GAG : generic address generator

GUI : graphical user interface

H

H : handle position, see definition 6-3, or
number of handle positions

HDL : hardware description language

HP : handle position, or
Hewlett Packard

HPG : handle position generator

HTML : hypertext markup language

I

iAGU	:	incremental address generation unit
ID	:	identity
IMEM	:	instruction memory
I/O	:	input / output
IOB	:	input output block
IOE	:	input output element
IP	:	intellectual property
IR	:	instruction register
IRMW	:	infrared missile warning
IS	:	instruction sequencer, or index stack
ISA	:	industry standard architecture

J

JPEG	:	joint photographic experts group
JTAG	:	joint test access group

L

L	:	Limit
L_0	:	initial Limit value
ΔL	:	step width for Limit modification
LAB	:	logic array block
LE	:	logic element
LIFO	:	last in first out
LSB	:	least significant bit
LSU	:	load and store unit
LSW	:	least significant word
LUT	:	look-up table

M

M : number of parallel memory banks

MAC : multiply/accumulate

MA-DPSS : multi architecture datapath synthesis system

MAG : memory address generator

MAP : memory access processor

MATRIX : multiple ALU architecture with reconfigurable interconnect experiment

MCU : move control unit

MDRAM : multibank dynamic read access memory

MemM : memory mapper

MIU : memory interface unit

MoM : map-oriented machine

MoM-PDA : map-oriented machine with parallel data access

MoPL : map-oriented programming language

MMU : memory management unit

MSB : most significant bit

MSW : most significant word

MUX : multiplexer

N

N : number of memory access cycles

NC : not connected

NN : nearest neighbor

NOP : no operation

O

OIB : operand instruction buffer

OP : operation

OS : operating system

P

PC : personal computer, or
program counter

PCB : printed circuit board

PCI : peripheral component interconnect

PCU : pipeline control unit

PDAS : perfect data access scheduling

PE : processing element

PIO : programmable input output

PISA : pixel oriented system for image analysis

PLCC : plastic leaded chip carrier

PLD : programmable logic device

PLL : phase-locked loop

POLU : problem-oriented logic unit

PQF : plastic quad flatpack

R

R : read

rALU : reconfigurable arithmetic logic unit

RAP : reconfigurable arithmetic processing

RAM : read access memory

rAP : reconfigurable arithmetic and logic unit port

RaPiD : reconfigurable pipelined datapaths

RC : reconfigurable cell

rDPU : reconfigurable datapath unit

RDRAM : Rambus dynamic read access memory

REG : register

RISC : reduced instruction set computer

rNN : reconfigurable nearest neighbor

RPU : reconfigurable processing unit

RR : reconfigurable resource

RS : read signal

RT : register transfer

RU : reconfigurable unit

R/W : read and write

S

S : scan step, see definition 6-5

SARAM : sequential access/random access memory, or single-access read access memory

SBS : software based sequencing

SC : control switch block

SD : data switch block

SDRAM : synchronous dynamic read access memory

SIM : sequencing and interface module

SIMM : single inline memory module

SMA : structured memory access

SMEM : switch memory

SoC : system on chip

SP : scan pattern, see definition 6-4, or stack pointer

SPACE : scalable parallel architecture for concurrency experiments

SRAM : static read access memory

SSCU : single step control unit

SW : scan window, see definition 6-2

SWG : scan window generator

SYS3 : systolic synthesis system

T

T : number of clock cycles

TI : Texas Instruments

TV : television

U

U : unrolling factor

URL : uniform resource location

V

VCC : Virtual Computer Corporation

VDAC : video digital analog converter

VHDL : VHSIC hardware description language

VHSIC : very high speed integrated circuit

VLSI : very large scale integration

VMEbus : versa-module european bus

VS : video scan

VSP : video signal processor

W

W : write, or
weight

WS : write signal

WWW : world wide web

X

X-C : Xputer C

XMDS : Xputer Multimedia Development System