

CALL FOR PAPERS

8th Reconfigurable Architectures Workshop (RAW 2001)

San Francisco, April 27, 2001

to be held in conjunction with

International Parallel & Distributed Processing Symposium (IPDPS 2001)

(sponsored by IEEE Technical Committee on Parallel Processing)

<http://www.ipdps.org/>

Note extended Submission Deadline – October 31, 2000

Note changed Workshop Date – April 27, 2001

The 8th Reconfigurable Architectures Workshop (RAW 2001) will be held at the San Francisco Airport Hyatt, April 27, 2001. RAW 2001 is associated with the 15th Annual International Parallel & Distributed Processing Symposium (IPDPS 2001, formerly IPPS & SPDP). RAW 2001 is one of the major meetings for researchers to present ideas, results, and on-going research on both theoretical and industrial/practical advances in Reconfigurable Computing.

Main focus of the Workshop

Run Time Reconfiguration - Foundations, Algorithms, Tools.

Reconfiguration of circuitry at runtime, also called run-time reconfiguration, is a new dimension in computing that blurs traditional barriers between hardware and software components. As a consequence, neither the processor architectures nor the hardware/software design methodologies and tools that are available today can fully exploit the possibilities created by this new computing paradigm. Algorithm designers and system designers alike are challenged to exploit the potential of innovative reconfigurable devices for the implementation and use of complex systems. This goal requires design tools based on a robust formal description of the underlying concepts of configurable computing in order to get independence from the frequently changing specific properties of commercially available devices. An appropriate combination of knowledge about dynamic reconfiguration technologies, the various different models of reconfigurable computing, programming methods, efficient algorithms, and the supporting tools, is required.

RAW 2001 is planned to provide a forum for creative and productive interaction between these disciplines, with a particular aim of encouraging the development of innovative algorithms targeted at novel reconfigurable systems.

Topics of Interest

Authors are invited to submit manuscripts of original unpublished research in all areas of run time reconfiguration (foundations, devices, systems, algorithms, software tools, and applications). The topics of interest include, but are not limited to:

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| + Reconfigurable Computing | + Programmable Logic Devices and Systems |
| - Models | - Reconfigurable Systems Architectures |
| - Algorithms and complexity | - Mobile circuitry |
| - Fault tolerance issues | - Evolvable hardware |
| - Configurable resource management | - Adaptable systems |
| + Development Tools and Methods | + Applications |
| - High-level design methods | - Mapping of parallel algorithms |
| - Compilation techniques | - Arithmetic/geometric/graph algorithms |
| - Support for virtual machines | - Wireless and distributed systems |
| - Methodologies and tools | - Industrial applications & experiences |

Authors should submit an electronic version of their work for review to Hossam ElGindy, University of New South Wales, Australia, hossam@cse.unsw.edu.au.

All manuscripts will be reviewed by at least three members of the program committee. Submissions should be a complete manuscript (not to exceed 8 pages of single spaced text, including figures and tables), or — in special cases — may be a summary of relevant work. Submissions should be in Postscript (level 2) format. Authors should make sure that the submission can be viewed using ghostscript and will print on a Postscript printer that uses standard letter size paper (8.5" x 11"). **Submissions must be received by October 31, 2000.**

In 2001, IEEE CS Press will publish the IPDPS symposium and workshop abstracts as a printed volume. The complete symposium and workshop proceedings will also be published as a CD-ROM disk.

Manuscript due	October 31, 2000
Notification of acceptance/rejection due	December 13, 2000
Final version due	January 20, 2001

Organization

Workshop Chair:	Hartmut Schmeck, University of Karlsruhe (Germany) schmeck@aifb.uni-karlsruhe.de
Steering Chair:	Viktor K. Prasanna, University of Southern California (USA) prasanna@ganges.usc.edu
Program Co-Chairs:	Gordon Brebner, University of Edinburgh (UK) gordon@dcs.ed.ac.uk Hossam ElGindy, University of New South Wales (Australia) hossam@cse.unsw.edu.au
Publicity Chair:	Oliver Diessel, University of New South Wales (Australia) odiessel@cse.unsw.edu.au

Program Committee

- Jeff Arnold, Adaptive Silicon Inc. (USA)
- Peter Athanas, Virginia Tech (USA)
- Gordon Brebner, Univ. Edinburgh (UK)
- Carl Ebeling, Univ. Washington (USA)
- Hossam ElGindy, Univ. New South Wales (Australia)
- Reiner Hartenstein, Univ. Kaiserslautern (Germany)
- Brad Hutchings, Brigham Young Univ. (USA)
- Mohammed Khalid, Quickturn Design Systems (USA)
- Hyoung Joong Kim, Kangwon National Univ. (Korea)
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- Martin Middendorf, Univ. Karlsruhe (Germany)
- George Milne, Univ. South Australia (Australia)
- Koji Nakano, Nagoya Inst. of Technology (Japan)
- Bernard Pottier, Univ. Bretagne Occidentale (France)
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- Jürgen Teich, Univ. Paderborn (Germany)
- Jerry Trahan, Louisiana State Univ. (USA)
- Ramachandran Vaidyanathan, Louisiana State Univ. (USA)
- Peixin Zhong, Lucent (USA)

Web Page: <http://www.cse.unsw.edu.au/~raw/>