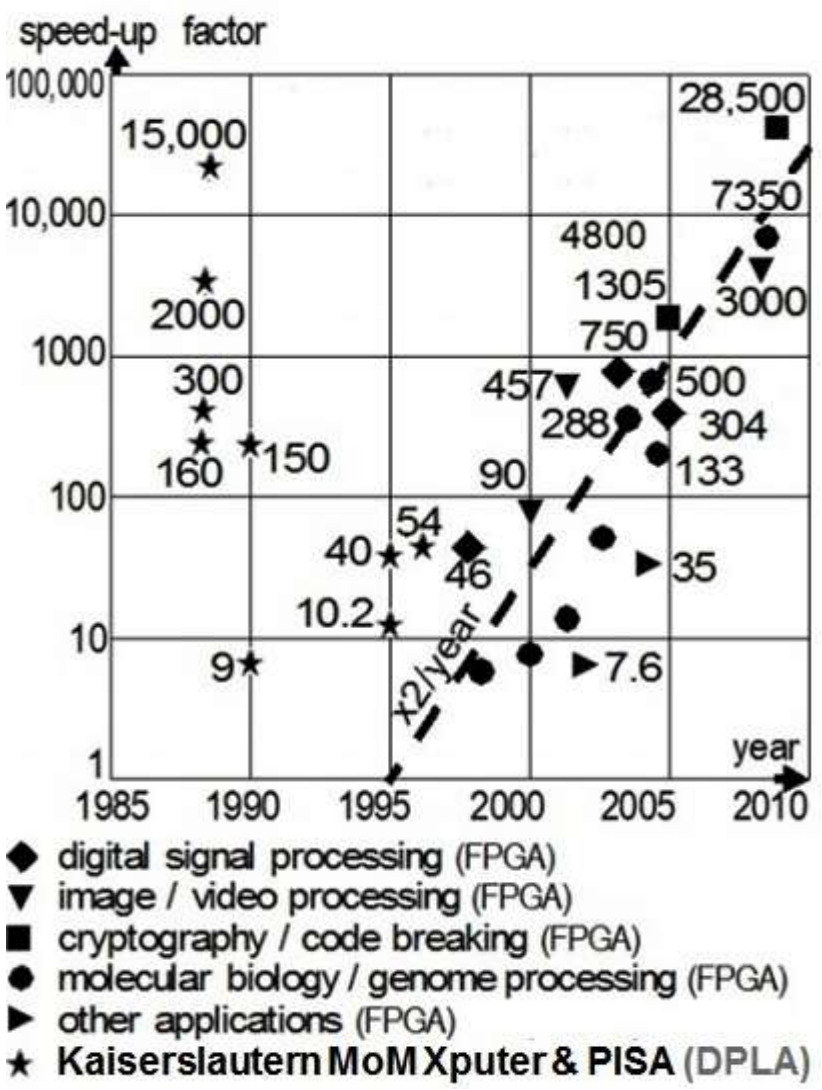
# Speed-up Factors

Reiner Hartenstein, Fb. Informatik,TU Kaiserslautern, IEEE fellow, FPL fellow, SDPS fellow http://hartenstein.de, April 2012




Compared to software implementations sensational speedup factors have been reported for software to configware migrations using FPGAs. Fig. 1 shows a few speed-up factors picked up from literature, reporting a factor of 7.6 in accelerating radiosity calculations [1], a factor of 10 for FFT, 35 for traffic simulations [2]. For a Lanman/NTLM Key Recovery Server [3] a speed-up of 50 – 70 is reported. Another cryptology application reports a factor of 1305 [5]. A speed-up factor of 304 is reported for a R/T spectrum analyzer [7]. In the DSP area [8] for MAC [8] operations a speedup of 100 has been reported compared to the fastest DSP on the market (2009 [9]). Already in 1997 versus the fastest DSP a speedup between 7 and 46 has been obtained [10]. In biology and genetics [11] a speedup of up to 30 has been shown for protein identification [13], by 133 [14] and up to 500 [15] in genome analysis, and 288 with the Smith-Waterman pattern matching algorithm at National Cancer Institute [17]. In the multimedia area we find factors ranging from 60 to 90 in video rate stereo vision [18] and in real-time face detection [19], as well as of 457 for hyperspectral image compression [20]. In communication technology we find a speedup by 750 for UAV radar electronics [21]. These are just a few examples from a wide range of publications [23] [24] [26] [27] [28] [30] [32] reporting much higher speedups, up to 28,500 [33] by FPGAs.

Energy-efficient computing is extremely important because of the declining world petroleum and gas supply [34 – 38, 54] and the growth rate of data stations and other communication technology equipment. By migration to reconfigurable computing the energy saving factor is roughly around 10% of the speed-up factor. [33] with a speed-up by 28.500 the electricity bill is divied by more than 4000. Before FPGAs came to market first field-programmable blocks from the early 80's have been so-called FPLAs featuring very area-efficient layout similar as known from ePROM memory for the price of being able to compute only Boolean functions in sum-of-product form. Very high speed-up could be obtained by matching hundreds of canonical boolean expressions within a single clock cycle instead of computing them sequentially by a microprocessor. Together with our reconfigurable address generator [34] this brought a speed-up by factor up to 15,000 [39- 43] for a grid-based design rule checker - already in the early 80's [44]. Via the multi project chip organization of the E.I.S. project such a FPLA (which was called DPLA) has been manufactured on a multi-project chip of the multi university E.I.S. project: the German contribution to the Mead-&-Conway VLSI design revolution [45] contributed by the PISA project [46]. This DPLA has the capacity of 256 first FPGAs (field-programmable gate array) just appearing on the market (by Xilinx in 1984). This also demonstrates the Reconfigurable Computing Paradox [46] (see section 2.3.2) Using a by orders of magnitude worse technology of FPGAs you obtain a speed-ups by several orders of magnitude (see the figure). This paradox demonstrates the unbelievably bad efficiency of the von Neumann machine paradigm. This is the secret of success by xputers: avoiding the von Neumann paradigm [47 – 53].

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[8] ***ASM*** = Auto-Sequencing Memory; ***DSP*** = Digital Signal Processing; ***EDA*** = Electronics Design Automation; ***ESL*** = Electronic System-Level Design; ***FIR*** = Finite Impulse Response; ***FPGA*** = Field-Programmable Gate-Array; ***MAC*** = Muliply and Accumulate; ***PU*** = Processing Unit ***rDPA*** = reconfigurable Data Path Array; ***rDPU*** = reconfigurable Data PathUnit; ***rE*** = reconfigurable Element

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