KressArray: what is the achievement ?

Generalization of the Systolic Array

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Rainer Kress describes a reconfigurable data path array [1-2] (KressArray [7-8]), which is a generalization of the systolic array. To map an application on a datapath array the traditional systolic array scene used algebraic synthesis methods based on linear projections, so that systolic arrays could be used only for applications with strictly regular data dependencies which yields only uniform arrays with linear pipes.

Kress removed these restrictions by discarding these algebraic synthesis methods and replacing it by simulated annealing implemented by his DPSS (data path synthesis system) mapper, so that reconfigurability makes sense. This means a generalization of the systolic array. So the KressArray supports also non-uniform arrays with a mix of different types of datapath units and any irregular and wild forms of pipes such as e. g. zigzag, spiral, feed-back loops, fork-and-join, and any other regular, irregular, and extremely irregular forms. Kress has been the first to publish a clear and simple partitioning scheme of the reconfiguration design flow into synthesis (configware implementation [9]) followed by data sequencing (flowware implementation [10])

The thesis of Rainer Kress includes only the description of a simple example of an array architecture. Another dissertation by Ulrich Nageldinger [3 - 6] covers the experimental exploration of the entire KressArray architecture design space by a design tool called KressArray Xplorer.

Literature*

***) also see:** *http://helios.informatik.uni-kl.de/staff/hartenstein/publications.htm*

[1] R. Kress: A Fast Reconfigurable ALU for Xputers, Ph. D. Dissertation 1996, Kaiserslautern University of Technology; available as a booklet only.

[2] R. Kress et al.: A Datapath Synthesis System for the Reconfigurable Datapath Architecture; Asia and South Pacific Design Automation Conference, ASP-DAC'95, Nippon Convention Center, Makuhari, Chiba, Japan, Aug./Sept. 1995

[3] U. Nageldinger et al.: Data Scheduling in Hardware/Software Co-Design for Field-programmable Accelerators; Proceedings of 7th International Workshop on Field Programable Logic, FPL`97, London, UK, September 1-3, 1997

[4] U. Nageldinger et al.: KressArray Xplorer: A New CAD Environment to Optimize Reconfigurable Datapath Array Architectures; 5th Asia and South Pacific Design Automation Conference 2000, ASP-DAC 2000, Yokohama, Japan, Jan. 25-28, 2000.

[5] U. Nageldinger et al.: Generation of Design Suggestions for Coarse-Grain Reconfigurable Architectures; Proc. Field-Programmable Logic and Applications (FPL2000), Villach, Austria, August 2000; Springer LNCS, 2000

[6] U. Nageldinger: Coarse-grained Reconfigurable Architectures Design Space Exploration; Dissertation, 2001, Kaiserslautern Univ. of Technology; downloadable via: http://xputers.informatik.uni-kl.de/papers/publications/NageldingerDiss.html

[7] http://www.fpl.uni-kl.de/staff/hartenstein/lot/Invent_something.htm

[8] http://kressarray.de/

[9] http://configware.org/

[10] http://flowware.net/

[11] for pdf files see: http://helios.informatik.uni-kl.de/staff/hartenstein/publications.htm

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