The Re-definition of Low Power Design for HPC: a Paradigm Shift

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Low Power Digital System Design has to be re-defined. Clever circuit level concepts to reduce leakage current effects etc. and to get along with a tiny battery have become lower-ranking. Slashing the electricity bill by up to millions of dollars has become the key issue - not only in High Performance Computing (HPC), e. g. also for server farms (for instance, Google's electricity bill amounts to about 50 million US-$/year).

Increasing the clock frequency of single-core microprocessors has come to an end. Multi-core microprocessor chips are not really the promising way to go for very high performance (vHPC). This lesson we have learnt from the supercomputing crisis, where the electric power bill is the most important obstacle on the way to obtain Petaflops by monstrous architectures having followed the wrong road map for decades. This problem can be solved only by a paradigm shift instead of circuit level issues.

For the solution we have to take a second look onto the Reconfigurable Computing Paradox. Although FPGAs have a substantially lower clock frequency, are power-hungry, are expensive, and their effective integration density is by 4 orders of magnitude behind Moore's law, the new road map is FPGA-based, it is based on the Reconfigurable Computing Paradigm. Software-to-Configware migration is the silver bullet to escape from the von Neumann paradigm trap for getting rid of the exponentially growing massive bottleneck problems coming along with traditional forms of increasing parallelism. Slashing the electricity bill is just a side effect of speedup factors having been published with up to 4 orders of magnitude.

The talk also explains the fundamental issues and bashes educational deficits cemented by newest CS-related ACM/IEEE-CS/AIS curriculum recommendations.